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Data Conversion With Subgate-Delay Time Resolution Using Cyclic-Coupled Ring Oscillators

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***Abstract*—An integrated circuit that measures time intervals with high precision and accuracy has a wide range of applications including data conversion, ranging, and 3D imaging. The resolution with which time intervals are quantized by a ring oscillator or delay line is limited by the minimum delay of an inverter in the technology. We propose the use of cyclic-coupled ring oscillators as a time-domain quantizer to achieve a combination of sub-gate-delay time resolution together with a short conversion time, thereby enabling data conversion with high resolution as well as high bandwidth. The resolution-power trade-off in coupled oscillators is studied. Simulation indicates up to a factor-of-13 sub-gate-delay time resolution with 13 coupled oscillators. A real-time quantizing time-to-digital converter with coupled oscillators is designed for a time-domain analog-to-digital converter. Powered by a factor-of-8 sub-gate-delay time resolution of 1.6 ps obtained with nine coupled oscillators, and a sample time of 4 ns for 11-bit conversion, the converter delivers a 9.9-bit ENOB over a signal bandwidth of 125 MHz and an SFDR of 88 dB. Results demonstrate that cyclic-coupled ring oscillators is an attractive candidate as a high-precision high-linearity time-domain quantizer for data converters.**

***Index Terms*—Time resolution, sub-gate-delay, time-domain, data converter, analog-to-digital converter, time-to-digital converter, oscillator, VCO-based ADC, ring oscillator, oscillator-based, technology-independent, cyclic coupled ring oscillator, CCRO, ADC, TDC, time-of-flight sensor, RADAR, LIDAR, ToF.**

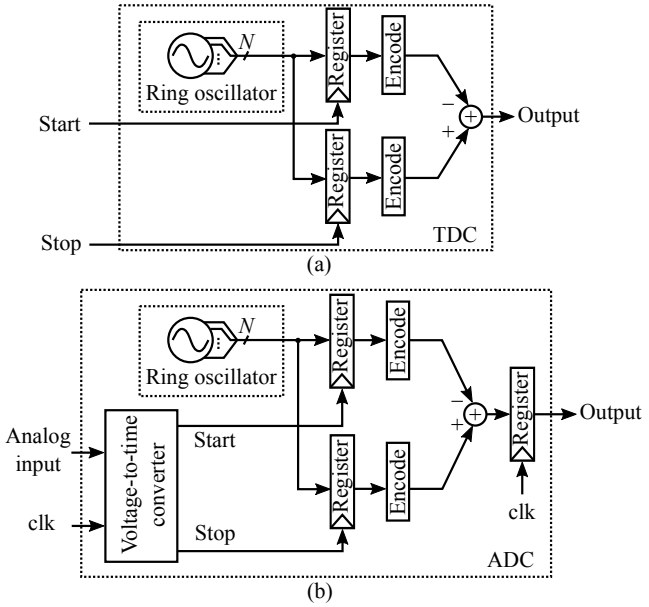

Fig. 1. Examples of oscillator-based data converters: (a) a time-to-digital converter, and (b) a time-domain ADC consisting of a voltage-to-time converter and a time-to-digital converter

I. Introduction

INTEGRATED circuits that measure time intervals with high precision and accuracy have a wide range of applications. They are used as a time-to-digital converter (TDC) in all-digital phase-locked loops and frequency synthesizers [1]. They are also applied as a time-of-flight (ToF) sensor in consumer- and automotive-grade radio or laser detection and ranging (RADAR/LIDAR) systems [2], nuclear instrumentation [3], and medical 3D imaging solutions [4]. An application that has recently gathered interest is time-domain analog-to-digital conversion [5], where time is utilized as a medium for signal representation instead of using voltage or current. The design of conventional analog-to-digital converter (ADC) architectures with voltage-domain or current-domain signal representation becomes increasingly difficult as semiconductor technology scales down into the nanometer regime, due to a the diminishing voltage headroom, and the decreasing intrinsic gain of the devices. Time-domain converters help circumvent the limitation by taking advantage of the increasing time resolution offered by nanometer-scale technologies to deliver a converter performance that improves with technology scaling. In addition, the energy and area efficiency of such converters are expected to improve with technology scaling similar to the case of digital circuits. Furthermore, time-domain signal representation enables an increased use of digital components thereby allowing improved design automation with computer-aided design (CAD) framework available for digital design hence reducing design effort relative to traditional full-custom analog design [6]–[9].

Majority of TDCs, time-domain ADCs, and ToF sensors employ a ring oscillator or a delay line as a time-domain quantizer [10]. Two examples of time-domain data converter circuits with ring oscillators are shown in Fig. 1. Fig. 1(a) shows a time-to-digital converter (TDC) where the progressive phase increment of a ring oscillator is used to quantize a time signal defined by the start and stop pulses. The blocks labeled encode convert the sampled phase of the oscillator into a numerical representation and the subtractor computes the difference between the samples. In Fig. 1(b), the same TDC operates as a part of a time-domain ADC where a voltage-to-time converter samples the analog input signal with a clock input to generate a proportional time-domain signal defined by the start and stop pulses. The time resolution

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in these converters is limited by the minimum delay of an inverter in the given technology. Most of the existing solutions to circumvent the limitation by enabling a sub-gate-delay resolution, such as the Vernier architecture [11]–[13] or the pulse-shrinking [14] architecture, increase the time required for quantization thereby limiting the sample rate and hence the bandwidth of the converter. Faster solutions such as voltage-domain delay interpolation fail to operate reliably across a wide range of switching characteristics [15]. Here, switching characteristic refers to the ratio of the propagation delay to the transition time.

In this work, we propose the use of cyclic-coupled ring oscillators (CCRO) as a time-domain quantizer to simultaneously obtain a sub-gate-delay time resolution together with a short conversion time. Further, a CCRO implements true time-domain delay interpolation, enabling reliable operation across a wide range of switching characteristics and hence across a wide range of process, voltage, and temperature conditions. The paper briefly reviews existing solutions to obtain a sub-gate-delay resolution in data converters. The use of CCRO as a signal quantizer is described and the resolution-power trade-off is studied by designing several coupled oscillator designs with a 28-nm CMOS process. Simulations indicate up to a factor-of-13 sub-gate-delay time resolution down to 0.39 ps while coupling 13 ring oscillators. A design example of a real-time quantizing TDC circuit, developed to be part of a time-domain ADC, is presented to illustrate the benefits of employing a CCRO as a high-precision high-linearity quantizer with sub-gate-delay time resolution. Powered by a factor-of-8 sub-gate-delay resolution of 1.6 ps when using nine coupled oscillators, and a 4-ns sample time for 11-bit conversion, the converter delivers a 9.9-bit ENOB over a signal bandwidth of 125 MHz as well as an SFDR of 88 dB according transistor-level simulation. The results demonstrate that a CCRO can operate as a high precision time-domain quantizer in data converters with high resolution and high sample rates.

The remaining part of the paper is organized as follows. Section II reviews existing solutions to obtain a sub-gate-delay time resolution in data converters. Section III presents an overview of CCRO and Section IV describes the use of CCRO as a time-domain quantizer. Section V presents a design example where a data converter with a CCRO is designed and simulated. Section VI concludes the discussion.

II. Sub-Gate-Delay Time Resolution: Prior Art

Several circuit techniques that achieve a technology-independent sub-gate-delay time resolution have been investigated with an aim of improving the resolution of time-to-digital converters. In the following subsections, a brief overview of these techniques is provided to place the proposed solution in context. Our aim is to achieve a robust high-resolution data conversion without compromising the signal bandwidth.

A. Conversion Time in Oscillator-Based Data Converters

The smallest quantization time-step in the converters in Fig. 1 is the smallest inverter delay possible in the given technology. Hence, the resolution of the converters is technology limited.

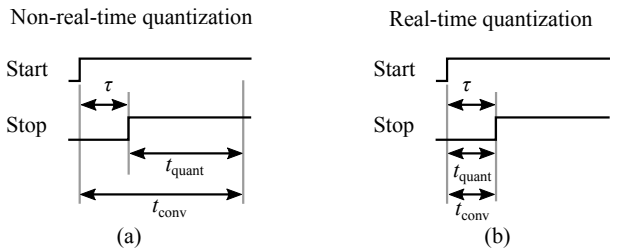

Fig. 2. Two types of time-to-digital converters: (a) non-real-time quantizing converters which quantize the target delay τ after the arrival of the stop signal and (b) real-time quantizing converters that quantize the delay between the start signal and the stop signal. Real-time converters are desired since they allow higher sample rates and conversion bandwidth.

The sample rate and hence the bandwidth of a converter is limited by the time required for signal quantization, t_{quant}. In a flash ADC with voltage-domain parallel quantizer, t_{quant} is independent of the resolution of the converter and is limited only by the time required for the quantizer circuit to settle. A synchronous successive approximation register (SAR) ADC where the signal is quantized sequentially by means of binary search has a t_{quant} linearly related to the converter resolution K. In a time-domain converter with ring oscillator or delay line quantizer, the signal is quantized by linear accumulation of quantization steps. Hence, the maximum t_{quant} is at least 2^K times the minimum time step, giving an exponential relation between conversion time and resolution. This significantly limits the sample rate and bandwidth of such converters. Time-interleaving is one solution to circumvent the limitation. Nevertheless, it is beneficial to reduce the conversion time of a single converter for a given resolution K. One way to achieve this is by improving the time resolution of the quantizer.

B. Conversion Time and Sample Rate in TDCs

Time-to-digital converters that measure the time τ elapsed between a start pulse and a stop pulse may broadly be grouped into two types: non-real-time quantizing converters that start quantizing the delay after the arrival of the stop signal and real-time quantizing converters that resolve the delay between the start signal and the stop signal. The time required for conversion in the former is illustrated in Fig. 2(a). The total conversion time is denoted by t_{conv}. The converter takes t_{quant} seconds after the arrival of the stop signal to finish the delay quantization. Hence, $t_{\text{conv}} = \tau + t_{\text{quant}}$. Note that t_{conv}, τ, and t_{quant} are signal dependent and their maximum value should be considered when determining the limitation on sample rate. Further, t_{quant} is exponentially related to the converter resolution K when measuring delays with delay lines as discussed in Section II-A. Conversion in a real-time quantizing converter that resolves the delay between the start signal and the stop signal is illustrated in Fig. 2(b). Since the conversion finishes at the arrival of the stop signal, $t_{\text{conv}} = \tau = t_{\text{quant}}$.

The conversion time t_{conv} is significantly shorter in real-time quantizing converters in relation to the other type, enabling higher sample rate and conversion bandwidth for a given

resolution. However, most of the conventional architectures that achieve a sub-gate-delay time resolution including the Vernier TDC and pulse-shrinking TDC are non-real-time converters. Non-real-time conversion may be acceptable in TDCs employed in phase-locked loops (PLL) since conversion is typically performed at the low reference signal frequency of the PLL. However, when designing high-performance data converters, real-time quantizing converters with a sub-gate-delay time resolution are desired to achieve a combination of high bandwidth and high resolution.

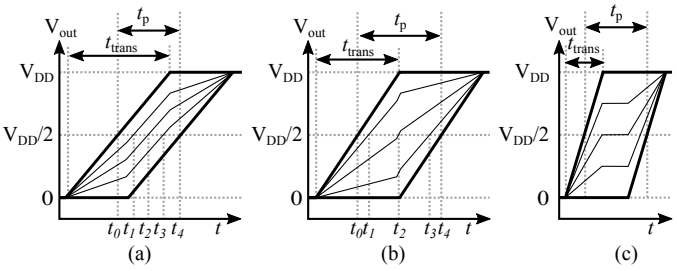

Fig. 3. Illustration of how passive/active voltage-mode interpolation fails to operate when the value of t_{p} exceeds the value of t_{trans} ($F = 4$).

C. Converters With Non-Real-Time Delay Quantization

This section briefly reviews major converter architectures with a sub-gate-delay time resolution and non-real-time delay quantization.

1) Vernier Measurement: In a Vernier TDC [11], [16], [17] the start signal is fed to a slow delay-line with an inverter delay of τ_1 and the stop signal is fed to a fast delay-line with an inverter delay of τ_2 ($\tau_1 > \tau_2$), hence obtaining a delay resolution with a step of $\tau_1 - \tau_2$. By setting $\tau_1 - \tau_2$ to less than the minimum gate-delay, sub-gate-delay resolution may be achieved. An area-efficient version with a ring structure is reported in [18] while architectures with first-order shaping of the quantization error are presented in [13], [19] achieving approximately up to 7-bit conversion over 800 kHz bandwidth.

2) Pulse-Shrinking: A pulse-shrinking delay line with unevenly sized inverters [14], [20], [21] achieves sub-gate-delay resolution since the width of a pulse passing through the boundary of two inverters with uneven drive-strengths reduces by an amount related to the asymmetry in the drive-strength. The technique achieves up to 9-bit conversion over 5 Hz bandwidth [14].

3) Time Amplification: A pipeline TDC employing a time amplifier circuit is reported in [22] achieving 11-bit conversion over 35 MHz bandwidth. Amplification of the target delay or the residual delay after a coarse stage of conversion, followed by quantization with minimum gate-delay may also be regarded as a technique to achieve sub-gate-delay time resolution.

D. Converters With Real-Time Delay Quantization

This section briefly reviews major converter architectures with a sub-gate-delay time resolution and a real-time delay quantization.

1) Passive Delay Scaling: Sub-gate-delay time resolution may also be achieved by scaling the load of a delay element with a configurable capacitor-bank [23]. However, it is difficult to design linearly distributed sub-gate-delays even with calibration of the passive elements, especially in nanometer processes where the gate-delay is around a few picoseconds and the wire-delay dominates over the gate-delay.

2) Passive and Active Delay Interpolation: Delay interpolation constructs sub-gate-delay transitions taking two transitions that are one gate-delay apart as the reference, which contrasts with delay scaling described above where only one transition is used a reference. Passive interpolation with resistors applied to a differential delay line [24], [25] achieves 7-bit conversion over 90 MHz bandwidth. An active interpolation circuit with voltage comparators proposed in [26] achieves around 9-bit conversion over 20 MHz. A similar technique is implemented with latches in [27], and an inverter-based interpolation circuit is presented in [28].

Note that both passive and active interpolation operates using voltage-domain comparison of the reference transitions. As a result, it fails to work when the transition time is short in relation to the propagation delay as described in [15]. This is illustrated in Fig. 3 with an example where the interpolation factor is four ($F = 4$). The propagation delay and the 0-100% transition time for an inverter are denoted with t_{p} and t_{trans} respectively. The bold lines in the figure show the reference transitions, while the thin lines show the interpolated transitions. When $t_{\text{trans}} \geq (1+(F-2)/F)t_{\text{p}}$, the interpolation works as intended (Fig. 3(a)). When $t_{\text{p}} \leq t_{\text{trans}} < (1+(F-2)/F)t_{\text{p}}$, interpolation works partially as it produces uneven delay steps (Fig. 3(b)). The interpolation fails when $t_{\text{trans}} < t_{\text{p}}$ as shown in Fig. 3(c) since it produces flat regions in the transition waveform [15].

3) Multi-Path Ring Oscillators: A ring oscillator where the i^{th} node is driven not only by an inverter whose input is connected to the $(i-1)^{\text{th}}$ node of the ring like in a regular ring oscillator but also by one or more inverters whose inputs are connected to other nodes of the ring is called a multi-path ring oscillator [29], [30]. A properly designed multi-path drive has the potential of achieving higher oscillation frequencies than what is possible with a regular ring oscillator. Hence, a multi-path oscillator may be regarded as a means to achieve sub-gate-delay time resolution. An error-shaping TDC employing a gated multi-path ring oscillator is reported in [31], [32] achieving 11-bit conversion over 1 MHz bandwidth.

4) Stochastic Interpolation With Ring Oscillators: A VCO-based converter that combines the phase output from a number of independent free-running ring oscillators is reported in [33] obtaining around 8-bit conversion over 100 MHz bandwidth. Since the relative phase alignment between individual oscillators is determined by a stochastic process, the improvement in resolution as a function of the number of oscillators is limited.

In this work, we present a solution that brings a significant improvement over stochastic delay interpolation with multiple ring oscillators. Instead of relying on stochastic distribution of the phases of individual ring oscillators, we employ cyclic-coupled ring oscillators where injection locking between the individual ring oscillators precisely controls their phases such

that the transitions are uniformly distributed in time, thereby bringing a significantly improved trade off between number of oscillators and phase resolution.

III. Cyclic-Coupled Ring Oscillators

The discussion in Section II implies that a real-time quantizing converter capable of resolving the target delay at sub-gate-delay time resolution with a robust delay interpolation technique is desired to achieve a combination of high resolution and high bandwidth. We propose the use of cyclic-coupled ring oscillators as a time-domain quantizer to achieve the same. Cyclic-coupled oscillators refers to an arrangement where a number of oscillators are coupled in a cyclic manner such that the phase relationship among the oscillators is precisely controlled by coupling. When ring oscillators with multi-phase output are cyclically coupled, the coupling forces the transitions in the oscillators to be uniformly spread in time, thereby generating a fine sub-gate-delay time reference. When a CCRO is employed as a quantizer in real-time quantizing converters like those shown in Fig. 1, the desired combination of both high resolution and high bandwidth is obtained.

A. Cyclic-Coupled Ring Oscillators

Multiple oscillators may be coupled in various configurations as shown in Fig. 4. The first generalized description of coupled array of ring oscillators can be found in [34], where the special case of cyclic coupling is mentioned. A more detailed analysis of cyclic-coupled ring oscillators is found in [35], where it is used for generating high frequency signals and for phase noise reduction. In this work, we apply cyclic-coupled ring oscillators as a time-domain quantizer in data conversion to achieve a combination of high resolution and high bandwidth as described in Section IV and Section V. Cyclic-coupled ring oscillators refers to an arrangement where a number of (say M) ring oscillators, each with N inverting delay elements, are coupled in a cyclic fashion like the configuration in Fig. 4(d) thus forming a ring of rings. We assume N and M are odd though this is not necessary when using differential delay elements. A 5×3 CCRO ($N = 5$, $M = 3$) is shown in Fig. 5 for a simple illustration. All inverters are realized with standard two-transistor inverter circuit in this work. The required unilateral coupling is achieved by means of the inverters labeled with 'c' connected between the respective nodes of the oscillators. The coupling inverters have a drive-strength k times the drive-strength of the inverters in the oscillators. CCROs are designed with $k < 1$ making the coupling inverters weaker than those in the oscillator. It may be noted that the coupling inverters also form five vertical ring oscillators that are cyclically coupled.

B. Operation

In the CCRO shown in Fig. 5, all the nodes of the horizontal oscillators are driven by the coupling inverters connected to the respective nodes of another oscillator in addition to the regular drive by the inverters within the oscillator. The coupling inverters thus implement a multi-phase injection-locking [36] between the adjacent ring oscillators. The injection-locking forces the coupled oscillators to arrive at a steady state (locked) where the oscillators maintain a certain phase relationship among themselves. By properly choosing N and M, that is by avoiding $N = M$, a uniform division of the phase into $2 \cdot N \cdot M$ phase steps can be obtained, thus achieving a factor-of-M improvement in phase resolution compared to a regular ring oscillator.

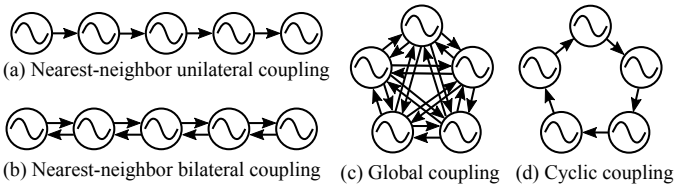

Fig. 4. Various configurations of coupled oscillators.

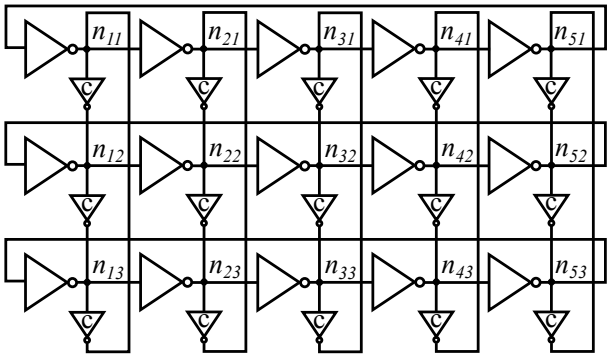

Fig. 5. A 5×3 cyclic-coupled ring oscillator.

C. Modes of Oscillation

The phase relationship between the oscillators when they are locked can have more than one solution, each of which corresponds to a mode of oscillation. A study on injection-locking in cyclic-coupled ring oscillators, and a preliminary analysis of the resulting modes of oscillation and their stability is available in [35]. For $k < 1$, the phase shift θ between any pair of adjacent nodes $n_{i,j}$ and $n_{i+1,j}$ in the horizontal oscillators has a single solution given by $\theta = \pi + \pi/N$. The phase shift ψ between any pair of adjacent nodes $n_{i,j}$ and $n_{i,j+1}$ in the vertical oscillators, however, has $M - 1$ possible solutions given by $\psi = n(2\pi/M)$ where n is an integer and $0 < n < M$. Each value of ψ represents a mode of oscillation. Certain modes are relatively more stable than the others and hence dominantly observed in a practical design. Further, M oscillators may oscillate in M distinct phases in certain modes while some of the oscillators may oscillate in-phase in other modes. The former set of modes is desired when using a CCRO as a phase-domain quantizer since it maximizes the phase resolution. A CCRO can be designed to oscillate in a desired mode (a mode that is stable and has maximal phase resolution) by properly setting N, M, and k as described in [35].

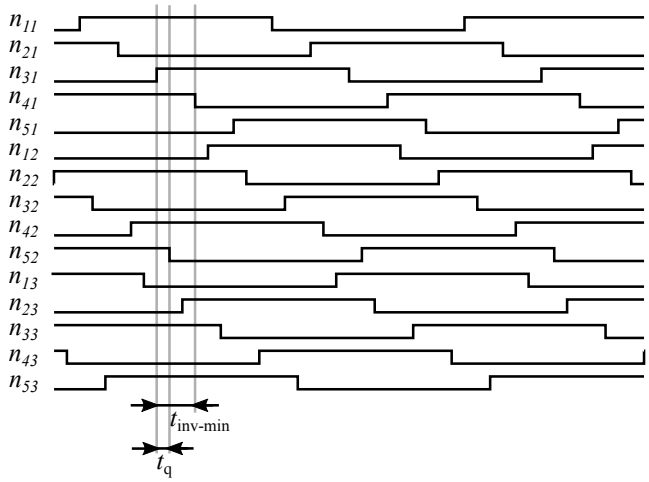

Fig. 6. The waveform at the multi-phase output of the CCRO in Fig. 5 for the mode with $\psi = 120°$. $M = 3$ yields a factor-of-three improvement in phase resolution.

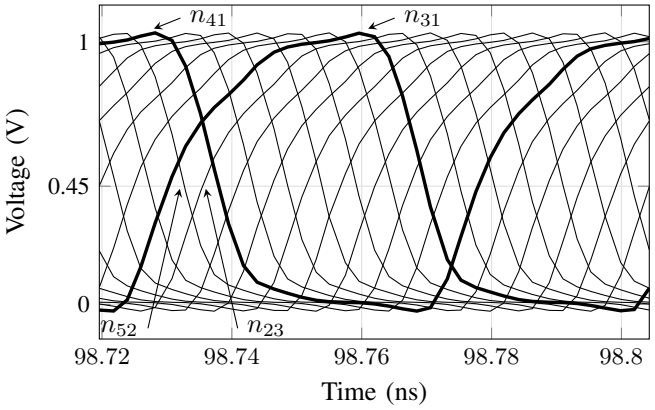

Fig. 7. Output waveform from transistor-level simulation of a 5×3 CCRO, demonstrating a uniform sub-gate-delay phase division at an effective switching threshold of 0.45 V. Two adjacent transitions of a horizontal oscillator are highlighted with bold lines, showing the two uniformly spaced additional transitions between them.

IV. CCRO AS A TIME-DOMAIN QUANTIZER

This section describes the use of a CCRO as a time-domain quantizer. Transistor-level simulation of several CCROs with varying dimensions designed with a 28 nm CMOS process is used for illustrations.

A. Sub-Gate-Delay Time Resolution

When a CCRO operates in a desired mode of oscillation where M oscillators oscillate in M distinct phases ensuring maximal phase resolution, it can be used as an efficient time-domain quantizer with a sub-gate-delay time resolution. This is illustrated in Fig. 6 which shows the waveform at the output of the CCRO in Fig. 5 when it oscillates in a mode that corresponds to $\psi = 120°$. Assume that the inverters in the oscillators are sized to obtain the minimal inverter delay (denoted by $t_{\text{inv-min}}$) for the given technology and the specific load conditions. It can be seen that the minimum time step t_{q} between the temporally adjacent transitions is $t_{\text{inv-min}}/M$. Hence, a sub-gate-delay time resolution (by a factor-of-M) is obtained with a CCRO, enabled by a factor-of-M improvement in phase resolution compared to a regular ring oscillator.

A 5×3 CCRO is implemented in a 28 nm CMOS process. The node voltages at the phase taps of oscillator obtained from a transistor-level simulation is shown in Fig. 7. The switching threshold of the inverters is around 0.45 V, which is marked with gray axis marker. A pair of temporally adjacent transitions in one of the horizontal oscillators is highlighted with bold lines, whose crossing with the switching threshold defines the delay of an inverter. It can be seen how injection locking adjusts the phase of individual ring oscillators such that two evenly spaced additional transitions are obtained between the above mentioned pair of transitions, thereby acieving a factor-of-three improvement in phase resolution and a sub-gate-delay time resolution.

B. True Time-Domain Delay Interpolation

Earlier reported time interpolation techniques in delay line structures with either passive or active interpolation operates in the voltage-domain, and hence fails to operate when the switching characteristics defined by the ratio $t_{\text{trans}}/t_{\text{p}}$ is small as illustrated in Section II-D2 (See Fig. 3). In contrast, cyclic-coupled oscillators implement a true time-domain delay interpolation by means of the injection locking between the oscillators. Hence, the time interpolation in a CCRO is expected to operate well across a wide range of switching characteristics defined by $t_{\text{trans}}/t_{\text{p}}$. Unlike voltage-domain delay interpolation techniques where the interpolated transition is defined by the interpolating circuits based on the instantaneous voltage of the reference transitions, true time-domain delay interpolation in a CCRO positions the robust transitions of individual ring oscillators by means of injection locking such that they are uniformly distributed in time.

C. Short Conversion Time and High Resolution

If the ring oscillator in the TDC architecture presented in Fig. 1(a) is replaced by CCRO, a sub-gate-delay time resolution and high sample rate is obtained. The arrangement forms a real-time quantizing converter with a short conversion time, as illustrated in Fig. 2 (Section II-B), in contrast with the existing solutions including the Vernier and the pulse-shrinking architectures that perform non-real-time quantization. Hence, the use of CCRO as a time-domain quantizer provides a relative advantage over conventional architectures in enabling data converters with a high resolution together with a high sample rate and bandwidth. The factor-of-M improvement in phase resolution obtained with a CCRO improves the converter resolution by $\log_2(M)$ additional bits compared to a ring oscillator. The improvement in resolution may alternatively be traded for a factor-of-M higher sample rate while maintaining the original resolution.

D. Phase Noise

A number of coupled oscillators have an increased collective momentum compared to a single ring oscillator. It is shown in [35] that this results in a reduction of phase noise by $10 \cdot \log(M)$ dB at the output of a CCRO. This is beneficial

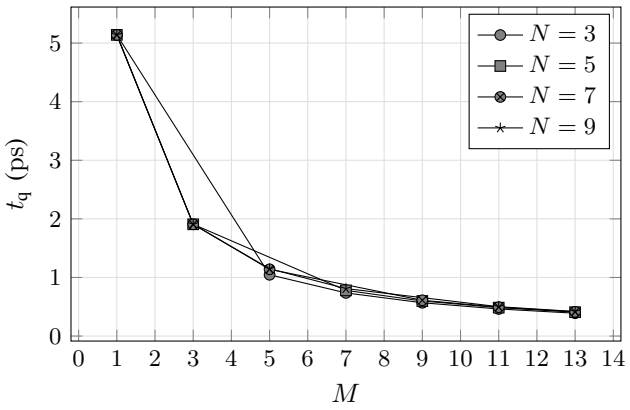

Fig. 8. Time resolution as a function of M for different values of N. $M = 1$ corresponds to a regular ring oscillator with same transistor dimensions and similar loading conditions as a CCRO.

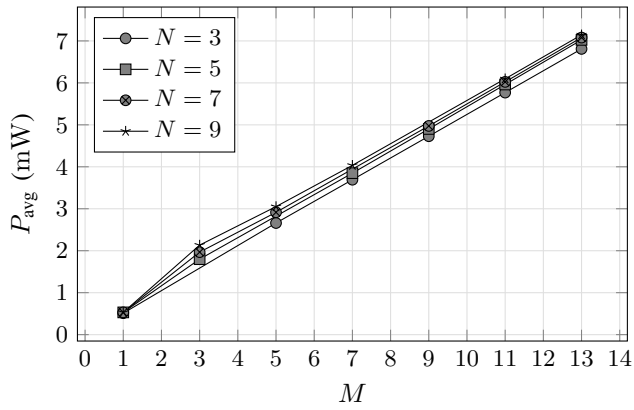

Fig. 9. Power consumption as a function of M for different values of N.

when a CCRO is used as a phase-domain quantizer in a data converter since the phase noise of the oscillator contributes to the conversion noise.

E. Frequency Deviation

The load and the drive seen at the nodes in a CCRO is higher than in a regular ring oscillator due to the coupling network. This, together with the injection locking mechanism, causes the effective $t_{\text{inv-min}}$ in a CCRO to deviate from $t_{\text{inv-min}}$ in a ring oscillator. This in turn causes the frequency of oscillation of a maximally fast CCRO to deviate from the frequency of a maximally fast ring oscillator (with same N) in a given technology. Further, the frequency of a CCRO is also dependent on the mode of oscillation. According to [35], the frequency of a CCRO is given by

$$w_{\text{CCRO}} = \frac{1}{RC}\frac{sin(\theta) + ksin(\psi)}{cos(\theta) + kcos(\psi)} \tag{1}$$

while that of the corresponding ring oscillator is given by

$$w_{\text{ring}} = \frac{tan(\theta)}{RC} \tag{2}$$

(obtained by setting $k = 0$). RC represents the passive load seen at the nodes. We can define a frequency deviation factor

$$F_\psi = w_{\text{CCRO}}/w_{\text{ring}} \tag{3}$$

to denote the mode-dependent frequency deviation.

F. Effective Time Resolution

The combined effect of the factor-of-M improvement in phase resolution and the frequency deviation determine the smallest time step t_{q} (LSB of the converter). In order to study the practical improvement in t_{q}, we designed several CCROs with varying dimensions (N, M) in a 28 nm CMOS technology. In the experiments, the length of the transistors in main and coupling inverters are set to 30 and 100 nm respectively, and the corresponding NMOS widths are set to 1.2 μm and 100 nm respectively. The transistor flavor is set to low-threshold-voltage. Since t_{q} is expected to improve with an increasing number of oscillators that are coupled, variation of t_{q} with M (for constant N) is studied. The variation of t_{q} as a function of M for different values of N, obtained from transistor-level simulation of the CCROs, is shown in Fig. 8. The data for $M = 1$ corresponds to a regular N-stage ring oscillator with transistor dimensions and loading conditions same as those of the oscillators in the CCRO. It can be seen that the CCRO achieves significantly smaller t_{q} compared to a regular ring oscillator thereby obtaining a sub-gate-delay time resolution. When $N = 3$, t_{q} for $M = 13$ is 0.389 ps in relation to the corresponding inverter delay of 5.14 ps, achieving approximately a factor-of-13 improvement in time resolution with 13 coupled oscillators. The time resolution improves with an increasing M as expected, with t_{q} diminishing in inverse proportion to M. Note that varying N does not have significant impact on t_{q}, since it is dependent on the CCRO frequency and total number of phases, both of which depend on N with opposite relationships. Thus, larger N will slow down the frequency of the CCRO and increase the number of phases in an equal manner resulting in constant t_q.

G. Short-Circuit Power

In a CCRO like the one shown in Fig. 5, nodes are driven by multiple inverters whose inputs may be at conflicting logic levels. This implies that there can be temporary conducting paths open between the supply and ground through a pair of series-connected NMOS and PMOS transistors, causing power consumption due to short-circuit current. Hence, the power consumption of a CCRO with M ring oscillators is expected to be larger than the power consumed by M regular ring oscillators.

H. Power Consumption

Average power consumption P_{avg} of a CCRO as a function of M for different values of N is shown in Fig. 9. It can be seen that the power consumption increases linearly with M for $M > 1$. Further, note that the power consumption increases also when N is increased while keeping M constant. However, the increase in power due to an increment in M is much larger than that due to an increment in N.

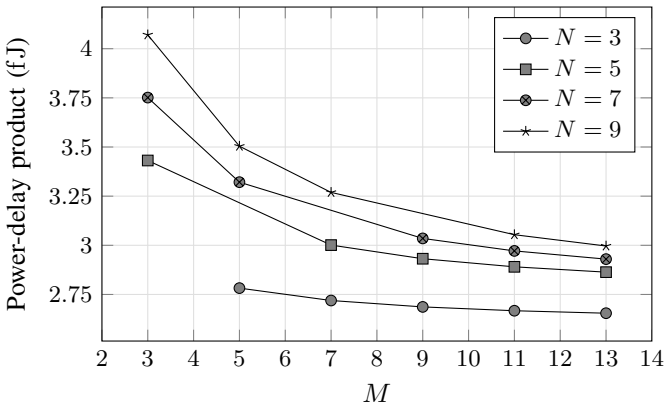

Fig. 10. Power-delay product ($P_{\text{avg}} \times t_{\text{q}}$) of the CCROs as a function of M for different values of N.

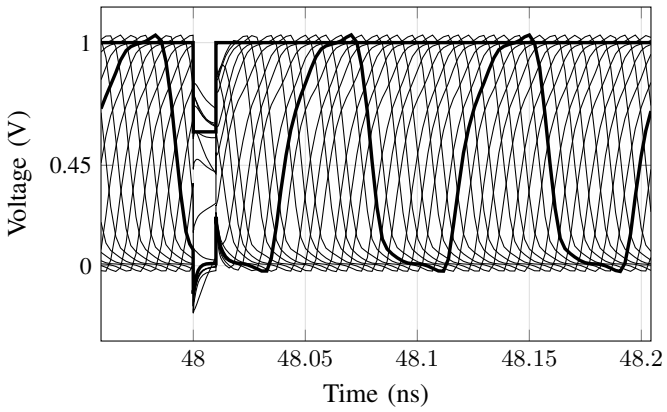

Fig. 11. Response of a CCRO to a 0.4 V drop in power supply for 10 ps, demonstrating the resilience of the phase relationship among the nodes to supply fluctuations. The uniform spacing of the transitions is restored within a couple of cycles. The supply voltage and one node voltage are highlighted with bold lines.

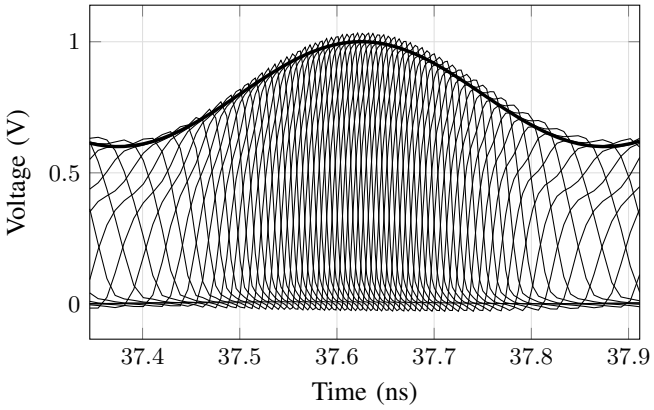

Fig. 12. Operation of a 5×3 CCRO as a supply controlled VCO, enabling its use in VCO-based ADCs.

I. Power-Delay Product

A short t_{q} together with a low power consumption is desired when a CCRO is used as a time-domain quantizer. From the discussion in Sections IV-A, IV-F, and IV-H, it follows that t_{q} decreases and power consumption increases in proportion to M. However, the scaling factor for the two dependencies can be different. Further, the effect of N in relation to M is unclear. Hence, we use the power-delay product, defined as the product of t_{q} and the average power consumption P_{avg} of the CCRO, to evaluate the power efficiency of a CCRO in creating sub-gate-delay resolution. A low value of power-delay product is desired since it corresponds to the energy consumption per transition. The power-delay product of a CCRO as a function of M for different values of N is shown in Fig. 10. For constant N, the power-delay product decreases with an increase in M since the reduction in t_{q} dominates over the increase in power. Another interesting observation is that a decrement in N for constant M also brings significant reduction in power-delay product. Hence, the trend in the power-delay product indicates that the energy-efficiency of the CCRO improves with decreasing N and increasing M. An intuitive circuit-level explanation for this trend can be done based on the short-circuit current discussed in Section IV-G. For constant M, increasing N only increases the number of nodes in the CCRO, and hence the total amount of short-circuit current that flows in the circuit. Note that increasing N does not bring any reduction in t_{q}. Hence, the power-delay product is lower for smaller N and constant M.

J. Resilience of Injection Locking to Supply Fluctuation

Robustness of the injection locking between individual oscillators is desired when coupled ring oscillators are used in data converters. The response of a 5×3 CCRO to an abrupt 40% reduction in supply voltage for a 10 ps duration is shown in Fig. 11. It can be seen that the initial mode of coupled oscillation with uniformly distributed transitions is restored within a couple of cycles, indicating good resilience of injection locking to supply variations.

K. Operation as a Supply-Controlled VCO

Fig. 12 shows the response of a 5×3 CCRO to a sinusoidal variation in supply voltage at 2 GHz. It can be seen that the uniform phase division that results from locked oscillation smoothly follows the variation in the frequency of oscillation. This enables the use of CCRO as a supply controlled VCO in VCO-based ADCs like the one in [5].

V. A Design Example

As an example to demonstrate the application of CCRO in data conversion, a 11-bit TDC is designed to be employed in a time-domain ADC like the one shown in Fig. 1(b), where a CCRO is used as a time-domain quantizer instead of a ring oscillator. It is simulated with a behavioral Verilog-A model of a voltage-to-time converter. The implemented circuit is shown in Fig. 13. The VTC model samples the analog input with the clock input. For each sample, it generates a pair of start and stop pulses which are separated by a time that is proportional to the sample.

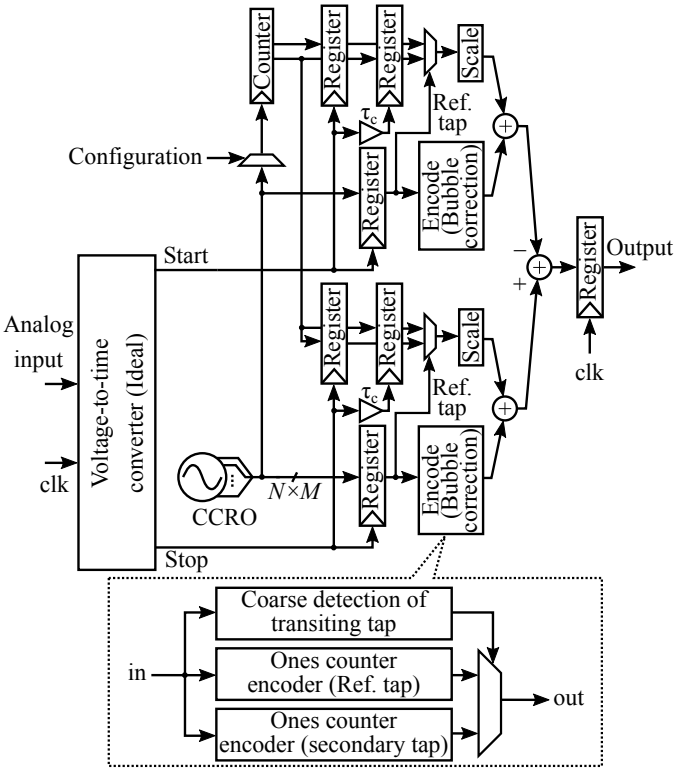

Fig. 13. Implemented circuit and the simulation set up.

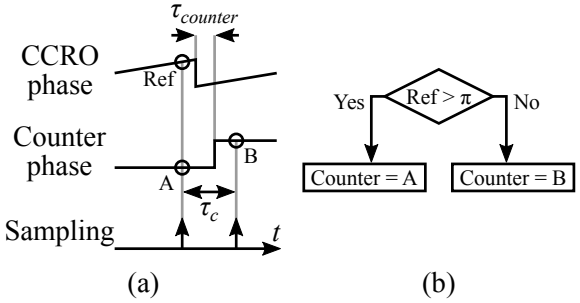

Fig. 14. Delayed double sampling of the counter phase (a) and selection logic for reliably selecting error-free counter samples (b).

A. TDC design with CCRO Quantizer

The TDC is a Nyquist-rate converter similar to the one in Fig. 1(a), where the oscillator operates at a fixed frequency providing a high resolution time reference for signal quantization. A CCRO is used instead of a ring oscillator. The CCRO is designed with $k = 0.025$. In addition, a high-speed synchronous counter, as presented in [5], is used to allow multiple CCRO cycles within a sample period. The dimensions of the CCRO is set as $N = 7$ (for proper counter operation) and $M = 9$ yielding $2\times N\times M = 126$ phase steps when rising and falling transitions are used (≈7-bit precision). A four-bit counter is used to extend the dynamic range of the converter to approximately 11 bits. The integer phase progression recorded at the counter and the fractional progression at the multi-phase output of the CCRO are sampled by both start and stop signals. The sampling registers consist of sense-amplifier flip-flops designed according to [37]. The sampled CCRO phase is encoded into a numerical representation using a ones counter -based encoder. The encoded phase of the CCRO sampled by the start signal is subtracted from the phase sampled by the stop signal to generate the digital output. The subtraction is performed in a wrap-around manner owing to the cyclic nature of the phase signal, according to

$$D_{\text{out}} = \begin{cases} D_{\text{stop}} - D_{\text{start}}, \text{ when } D_{\text{stop}} \geq D_{\text{start}}, \\ D_{\text{stop}} - D_{\text{start}} + 2^C \cdot 2NM, \text{ otherwise}, \end{cases} \tag{4}$$

where D_{start} and D_{stop} are the encoded start and stop channel samples, respectively, C is the bit depth of the counter, and N and M are the dimensions of the CCRO.

The CCRO, counter, and the sampling register has numerous sources of circuit non-idealities, and demands careful design to minimize errors. The systematic circuit imperfections contributing to the phase-domain errors in the samples include delay cell mismatch in the CCRO, mismatch in the wiring between multiple taps of the CCRO and the register, and the clock skew within the register. All these effects can be modeled together as one delay mismatch in the phase signal. When the magnitude of net delay mismatch approaches and exceeds an LSB of the converter, large conversion errors can results. The proposed design has several features that builds robustness to large conversion error arising from the mechanism described above, as well as other design specific circuit imperfections. Specific design features and related details are described in the following subsections.

1) Coherent sampling of integer and fractional phase progression: The sampling of the integer phase progression at the counter and the fractional phase progression at CCRO output should be done in a coherent way in order for the sampling to be robust to delay mismatches in the layout, and to avoid large conversion errors resulting from the same. We achieve this with a solution similar to the one described in [38]. The counter output is double sampled by two registers that are triggered with a constant delay between them, τ_{c} as shown in Fig. 14(a). The phase tap of CCRO that is connected to the counter is selected with a configuration as shown in Fig. 13, allowing the effective counter delay τ_{counter} to be tuned. The selection is carried out by a tree of cascaded OR-gates forming a 63-to-1 multiplexer. One among the two samples is chosen based on the value of the sampled reference tap of the CCRO as presented in Fig. 14(b). The double sampling correction is based on the fact that both integer and fractional samples capture the same circuit event in the CCRO, which allows for them to be aligned post-sampling [39]. When the adjustable delay between the two counter samples is sufficiently larger than the cumulative CCRO-to-counter delay ($\tau_c > \tau_{\text{counter}}$) and shorter than half-period of the CCRO ($\tau_c < T_{\text{CCRO}}/2$), one of the counter samples is guaranteed to be error-free in all cases. This will effectively align the sampled integer and fractional phases.

2) Bubble error mitigation: The sampling of the multi-phase output of the CCRO requires extra care since transition reordering can occur when the delay mismatch among the phase taps approaches and exceeds the t_{q} of the converter.

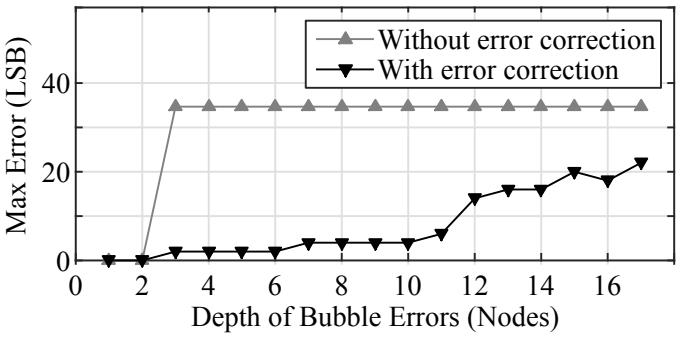

Fig. 15. Simulated demonstration of the robustness of the bubble error suppression logic to arbitrary reordering patterns as indicated by the maximum encoding error plotted against the number of taps on which the bubbles are spread, for the example of a six-bit encoder. Each data point is simulated with a large number of test vectors with random bubble patterns.

The mismatch may arise from nonuniform loading of the taps as well as from timing skew within the sampling register. The mismatch problem becomes particularly aggressive when using a CCRO instead of a ring oscillator, since the sub-gate-delay t_q enters the picosecond-range. A solution similar to our earlier work [40] with ring oscillators is employed to suppress bubble errors in the sampled fractional phase, as shown in Fig. 13. It employs two ones counter encoders operating with two reference taps separated by approximately $\pi/2$ phase shift, to provide a very effective pattern-independent bubble suppression as described in [40]. Simulated demonstration of the robustness of the bubble error suppression logic to arbitrary reordering patterns is illustrated in Fig. 15, where maximum encoding error is plotted against the number of taps on which the bubbles are spread, for the example of a six bit encoder. Each data point is simulated with a large number of test vectors with random bubble patterns. It can be seen that the logic provides effective suppression against arbitrary patterns that may arise from layout-induced delay mismatches and skew within registers, which are otherwise difficult predict. The maximum encoding error is significantly low for a wide range bubble depths, compared to the case without bubble error suppression.

3) Inherent dynamic element matching: Since the CCRO runs asynchronously in relation to the start signal, each delay measurement starts at a position in the ring that can be different from the start position for the previous measurement. This contrasts with a linear delay-line where every measurement starts from a fixed delay-element. The inherent cycling of the delay elements from sample-to-sample implements a dynamic element matching (DEM) of the delay-elements and hence reduces the spurious tones generated due to the nonlinearity arising from the delay mismatch among the delay-elements. Hence, the architecture has inherent DEM that relaxes the accuracy requirement regarding the matching of delay stages in the CCRO.

4) Metastability: Asynchrony between transitions in the CCRO and sampling clock implies that there is a possibility of sampling circuit entering metastable state. As a crucial design strategy to deal with metastability, we have designed the sampling register with high gain such that the metastability recovery time is reduced. If it can be assumed that the metastability does not spread into other circuits, and that the value of the affected node is interpreted by the reading circuit as any valid value, metastability does not cause additional conversion error if the design ensures monotonous accumulation of LSBs [5]. In the proposed design, the unit-distance cyclic block code inherently present at the CCRO output, and the coherent sampling of integer and fractional phase progression described in Section V-A1 ensures monotonous increment of LSBs. Further, the bubble error mitigation described in Section V-A2 ensures monotony in LSB accumulation even in the presence of transition reordering errors arising from delay mismatch.

5) Implementation: The TDC is implemented at transistor-level with a 28 nm bulk CMOS process. The CCRO, counter, multiplexer and sampling flip-flops are custom transistor-level designs. The remaining sections of the TDC are synthesized from a VHDL description using vendor-provided standard cell libraries. The area estimate for the synthesized part is around 1790 μm^2. The mismatch modeled in the design include the load mismatch at the oscillator output caused by connecting the counter, and the back-referred timing skew within sampling registers caused by the load imbalance at the register output due to the connection to the encoder and multiplexer control as shown in Fig. 13.

TABLE I
SIMULATED PERFORMANCE OF THE CONVERTER.

Metric	Performance
Sample rate (MHz)	250
Signal bandwidth (MHz)	125
LSB size (ps)	1.64
Resolution (bits)	11
DNL (LSB)	[-1.00, +1.42]
INL (LSB)	[-1.06, +0.94]
Linear bits [1]	9.96
SNDR (dB)	61.4
ENOB (bits)	9.9
SNR (dB)	61.5
SFDR (dB)	88.1
THD (dB)	-83.71
Power (mW)	7.13
FoM_1 [2] (fJ)	30.1
FoM_2 [3] (fJ)	28.5

[1] Linear bits = Resolution - $\log_2$(INL+1)
[2] FoM_1 = Power/(Sample rate$\times 2^{\text{ENOB}}$)
[3] FoM_2 = Power/(Sample rate$\times 2^{\text{Linear bits}}$)

B. Simulated Performance

Transistor-level simulations are performed with transient noise to evaluate the performance of the converter. The converter is clocked at 250 MHz and excited with a 2 MHz single-tone input.

The performance of the converter is summarized in Table I. A sub-gate-delay resolution with an LSB of 1.64 ps is obtained, which is approximately factor-of-8 (note $M = 9$)

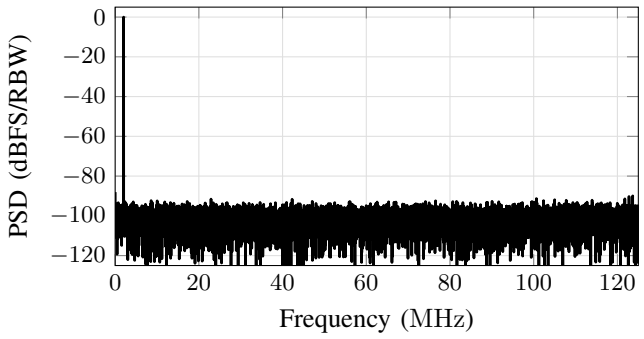

Fig. 16. Spectrum of the converter output for a single-tone test with an input frequency of 2 MHz obtained from transistor-level simulation with device noise enabled. The sample rate is 250 MHz.

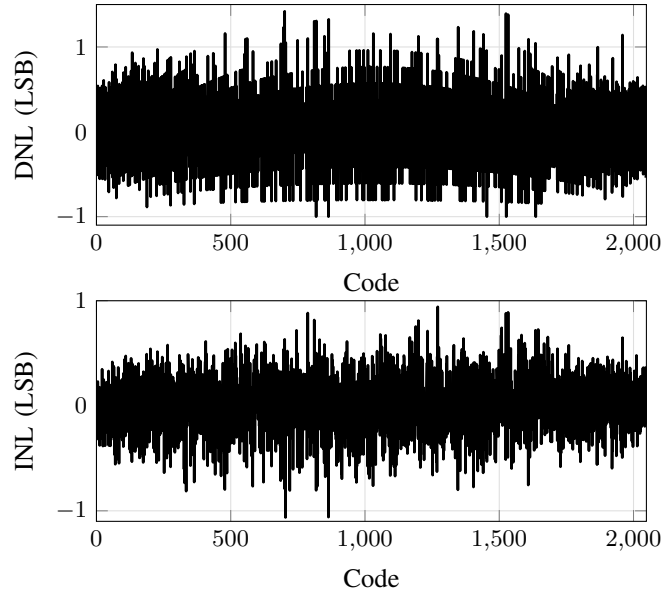

Fig. 17. DNL and INL of the converter.

finer than the inverter delay of 13.2 ps observed for the loading conditions in the circuit. The spectrum of the output computed from 2^{14} samples is shown in Fig. 16. The converter exhibits good linearity with no significant harmonic distortion or other distortion tones dominating the noise floor. An SFDR of 88.1 dB and a THD of -83.7 dB confirms the good linearity performance. Further, the DNL and INL of the converter are estimated from the single-tone response using the histogram method. The DNL and INL are plotted in Fig. 17, which also indicate good linearity performance in agreement with the dynamic metrics. The DNL and INL are [-1.00 +1.42] and [-1.06 +0.94] respectively. Further, the converter delivers a 9.9-bit ENOB (61.4 dB SNDR), and a 61.5-dB SNR over a 125-MHz signal bandwidth.

A DC test is performed to evaluate the single shot precision of the TDC. The histogram of the converter output from around 4000 samples for a DC input at low, mid, and high codes are plotted in Fig. 18, and the respective standard deviations are 0.54 LSB, 0.67 LSB, and 0.60 LSB.

The power consumption from a 1 V supply is 7.1 mW, resulting in an energy efficiency (Walden FoM) of

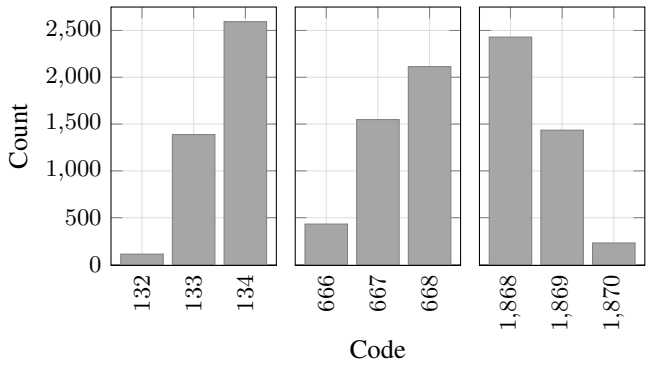

Fig. 18. Single shot precision illustrated by the histogram for low, mid, and high codes. The respective standard deviations are 0.54 LSB, 0.67 LSB, and 0.60 LSB.

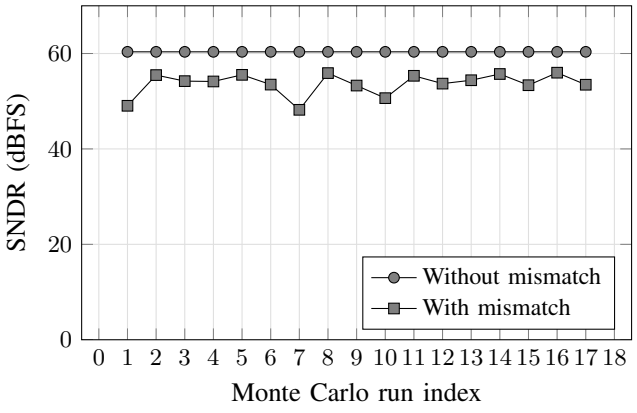

Fig. 19. Monte Carlo simulation result demonstrating the variation of performance in the presence of process mismatch.

30 fJ/conversion step. Note that the power and FoM estimates apply to the TDC since the power consumption of the VTC is not included.

A Monte Carlo simulation is performed on the converter circuit to evaluate the impact of process mismatch. The result is shown in Fig. 19, where the SNDR with and without mismatches is plotted against Monte Carlo run index.

C. Suppression of Phase Noise

Since the transistor noise is enabled, the simulation provides an estimate of the phase noise of the oscillator. Simulated phase noise of the CCRO and a ring oscillator with inverters of same transistor dimensions is shown in Fig. 20, which indicates more than 11 dB lower phase noise with the CCRO. The accumulated phase noise from up to 2^{11} transitions in the oscillator ($K = 11$) can be present in each sample. Note that the phase noise is not accumulated across samples since each sample is computed with the difference operation between a new pair of start and stop samples (See Fig. 13) which are uncorrelated to the previous phase samples. While the phase noise accumulation within each sample (with up to 2^{11} accumulated LSBs) can cause significant conversion noise with a regular free-running ring oscillator, the converter delivers a relatively good SNR of 61.5 dB over a signal

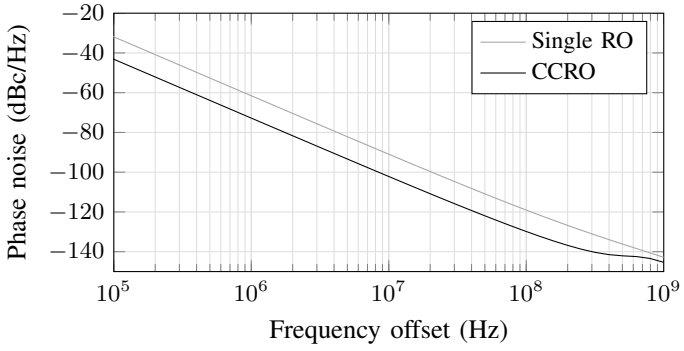

Fig. 20. Simulated phase noise of the CCRO and that of a ring oscillator with inverters of same transistor dimensions. Phase noise is reduced by more than 11 dB with CCRO.

bandwidth of 125 MHz compared to the ideal 11-bit SNR of 67.98 dB (Calculated with SNR $= 6.02 \times K + 1.76$ dB). This shows the effectiveness of the CCRO in suppressing the phase noise compared to a regular ring oscillator, leading to an improved noise performance in oscillator-based converters.

VI. Conclusion

The paper proposes cyclic-coupled ring oscillators as a time-domain quantizer in data converters to obtain a technology-independent sub-gate-delay time resolution together with a short conversion time thereby enabling high sample rate and conversion bandwidth without compromising resolution. Resolution-power trade-off in the design of CCROs is studied. Results demonstrate that coupling a large number of oscillators, where each oscillator has a small number of inverters, is favorable for high energy efficiency. Simulation indicates a factor-of-13 sub-gate-delay time resolution of 0.389 ps when using 13 coupled oscillators. A real-time quantizing TDC circuit is designed with a 28-nm CMOS process, where a CCRO operates as a quantizer. The converter delivers a 9.9-bit ENOB over a signal bandwidth of 125 MHz as well as an SFDR of 88 dB according transistor-level simulation. The results demonstrate the operation of CCRO as a high-linearity sub-gate-delay resolution time-domain quantizer in high-performance data converter circuits. In addition to data conversion, the circuit idea presented may easily be extended to any high-precision time measurement application including ToF sensors employed in RADAR and 3D imaging systems.

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