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A 5.4-GHz 2/3/4-Modulus Fractional Frequency Divider Circuit in 28-nm CMOS

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***Abstract*—This paper describes the design and post-layout simulations of a 2/3/4- modulus frequency divider circuit, accompanied with an accumulator that controls the division count. The circuit is capable of operating as an integer or as a fractional divider. Key topic of this paper is the merging of div-2/3 and div-3/4 circuits into a single compact circuit that solves an issue of a forbidden state in fractional-division operation. The circuit is designed with 28-nm CMOS technology and the post-layout simulations indicate an operating input frequency range of 0.3 – 5.4 GHz with 13-bit fractional frequency resolution between division ratios of 2–4. The divider occupies only 40 µm x 30 µm while consuming 2.0 mW at 5.4 GHz input frequency.**

***Index Terms*—Frequency division, frequency synthesis, CMOS, RFIC**

I. Introduction

Frequency synthesizers are one of the key blocks in most telecommunication systems. Synthesizers for advanced System-on-Chip implementations need to support various bands and multiple clock domains for digital signal processing. A sophisticated method for generation of these frequencies with minimum silicon area, power consumption, and degradation of signal quality is of uttermost importance. Typically, a single highly precise frequency reference, such as a crystal oscillator, is applied, and indirect frequency synthesis via fractional-N phase-locked loops is ubiquitously used for high-frequency signal generation. Recently, there has been research activity to further improve the frequency range, resolution, and settling time of such frequency generation by using fractional frequency dividers [1]–[6] and multipliers [7]–[10].

Fractional frequency division is based on altering the division count of an integer divider in a continuous manner. Typically, a $\Sigma\Delta$-modulator is used for this [11]. Features of the integer-N divider with variable division count N, i.e. a multi-modulus divider, sets the overall performance of such an entity. In this paper, a new multi-modulus 2/3/4- frequency divider circuit is presented. The circuit can act as a stand-alone divider or as a part of a larger frequency synthesis circuit. The circuit is based on known divide-by-2-or-3 (div-2/3) and div-3/4 circuits [12] that are depicted in Fig. 1. We propose a new feedback structure that enables modulus-2/3/4 operation and solves an issue of a forbidden state in the fractional-division operation, while occupying a smaller die area than two separate dividers.

The paper is organized in the following way: Section II describes the fractional division concept employing the averaging of integers, and then presents the issue of forbidden states,

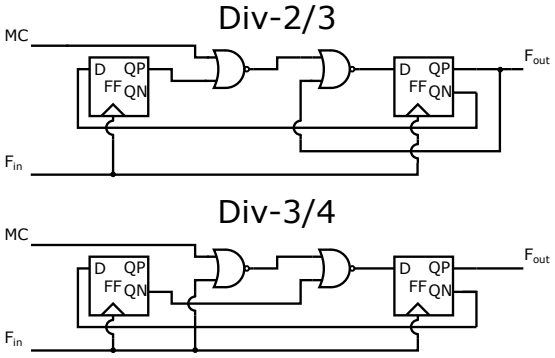

Fig. 1. Block diagrams of 2-or-3 and 3-or-4 divider configurations.

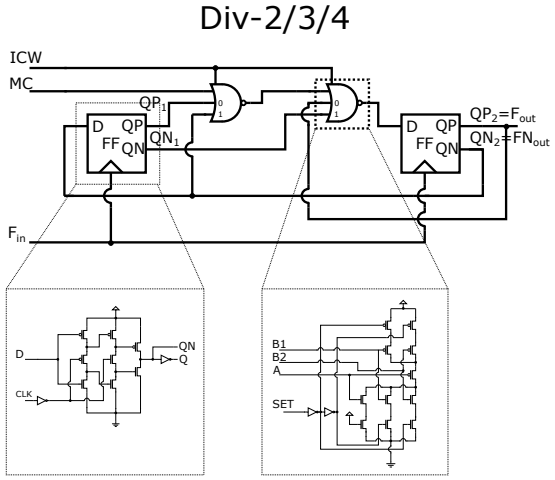

Fig. 2. Block diagram of the proposed multi-modulus frequency divider with transistor level implementations of the main components.

Section III introduces the proposed multi-modulus frequency divider, Section IV describes post-layout simulation results, and Section V concludes the paper.

II. Fractional Frequency Synthesis with Integer Divider Circuit

Fractional frequency synthesis is a process of generating signals with a fractional value relation to a known input frequency signal. One method for non-direct fractional frequency synthesis is the use of time-averaging processes with multi-modulus dividers [2]. Averaging in terms of frequency synthesis is the approximation of a fractional value with the

use of controllable switching of integer division ratios. The averaging occurs in time domain as the ratio of two integer values is varied proportionally in time. In frequency synthesis context this method is known as $\Sigma\Delta$-modulation [11].

Fractional frequency synthesis requires two features to be fulfilled when the method is based on time-domain averaging. The features are: distinct integer division ratios and book-keeping of the enable ratios between division ratios. These features are achieved with an instantaneously switchable multi-modulus divider (MMD) and an accumulator. The MMD is responsible for generating the proper pulse ratios corresponding to a given division ratio, whereas the accumulator is responsible for keeping record of the enable ratio between two integer division values as per the following equation

$$\begin{aligned} N_{frac} &= \frac{X}{X+Y} \cdot N + \frac{Y}{X+Y} \cdot (N+S) \\ &= N + \frac{Y}{X+Y} S, \end{aligned} \tag{1}$$

where N_{frac} is the fractional division ratio formed by averaging integers N and N+S in a specific ratio formed by X and Y. S is the step size between the integer ratios which is typically one. With $S = 1$, the fractional part of the division ratio is defined by the book-keeping circuit i.e. the accumulator. In other words, the fractional division ratio achieved with the averaging method shifts the fractional resolution from the divider circuit itself into the circuit corresponding to the control of the division ratio of the MMD. The controlling circuit consists of the accumulator and logic gates that are compatible with the modulus control logic of the MMD. Precise generation of the control signal is crucial for defining the achievable fractional resolution and the divider also has to be capable of switching the division ratio fast enough in order not to cause glitches to the output signal.

A. Instantaneous Switching

Instantaneous switching in the context of an averaging fractional frequency divider means that the modulus control signal is adjusted during the logic level at which the MMD output is not affected. The output is required to be stable as the accumulator and the corresponding modulus control (MC) logic is clocked using an iteration of the MMD output signal, such as a delayed version of the output signal.

Instantaneous switching without glitching is reliant on choosing the proper trigger signal for the MC logic. Usually the trigger signal is a one-input-pulse delayed version of the MMD output signal. The delayed version of the signal includes sufficient information on what the internal states of the MMD are, and thus the probability of glitching during switching operation can be reduced with careful design.

Knowledge on the internal states of the MMD is required for deciding the specification of the trigger signal, such as which edge of the delayed MMD output signal to use. Internal states and transitions between division ratios can be illustrated with a state diagram depicted in Fig. 3. The diagram specifically

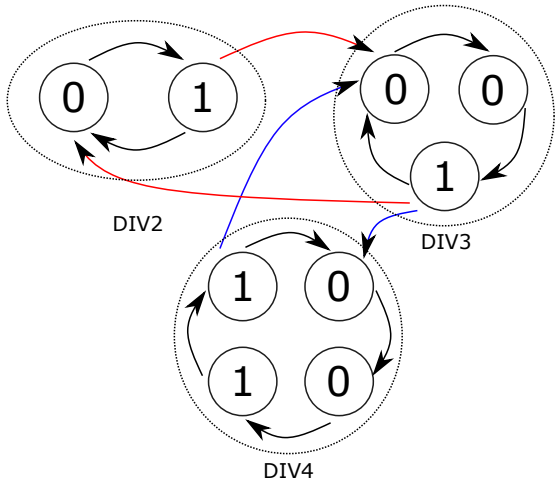

Fig. 3. State diagram of the multi-modulus divider output for integer divisions of two, three and four.

demonstrates the fractional division operation between integer ratios of 2–4. Within the diagram, the low state is represented with ”0” and the high state with ”1”. The arrows with black tails represent the arrival of a rising/falling edge of the to-be-divided input signal, whereas the colored tails represent the transitions between integer division ratios for producing average fractional values. Observing the state diagram of Fig. 3, it is apparent that the number of internal states will be different for a given division ratio from two to four. Thus it is important to choose the proper point for switching between division ratios for fractional frequency division operation.

B. Forbidden States in Fractional Dividers

Instantaneous switching is a dynamic operation which can result in a deadlock situation within the MMD. Synchronous MMDs are designed with flip-flops and various combinations of combinational logic. The arrangement of the combinational logic will decide the value of the division ratio and the number of possible division ratios. For a given integer division ratios, there are multiple combinational logic arrangements that can provide the desired division ratio. The versatility is both an opportunity and a challenge.

The state diagram in Fig. 3 represents the output of the MMD, and it is valid for all types of MMD regardless of the implementation. The challenge in the number of feasible MMD implementations is that there might be internal forbidden states in the MMD. These forbidden states might not be present in integer division mode, but could appear during improper switching in fractional division mode. Switching operation that leads to an internal deadlock state of the MMD must be avoided with proper circuit design.

The method for avoiding internal forbidden states in a MMD starts by evaluating the logical combinations present at the logic gate which is connected to the flip-flop corresponding to the output of the MMD. Then it is necessary to understand how this signal propagates through the flip-flops back to the said logic gate. If any combination of logic states at the flip-

flop output node leads to no change in the logic gate, there is an inherent forbidden state. In such cases, the problem can be circumvented by changing the combinational logic with an alternate implementation for the desired division ratios and then re-evaluating the presence of forbidden states again.

III. Proposed Multi-Modulus Frequency Divider

Our primary goal is to develop a compact, low-power and wideband fractional divider, and for this purpose we need a div-2/3/4 circuit. Multi-modulus divider circuits are based on static integer dividers with additional combinational logic applied to them for achieving various lower division ratios. The setting of the combinational logic will determine the division ratio as well as the critical timing path. These design parameters in turn will limit the feasible operating frequency range.

Two prior alternatives for a div-2/3/4 circuits are to simply have div-2/3 and div-3/4 circuits in parallel, or a prior art circuit [2] depicted in Fig. 4. The first alternative suffers from extra die area, larger load at the input due to additional flip-flops, and additional complexity for changing operation modes with either multiplexer setup or by turning on/off the parallel branch. We observed that the second alternative has one shortcoming, which is the presence of a forbidden state in division by 3. The forbidden state is present due to the use of a XNOR gate, which can get stuck given the $MC<1:0>$ is set to 11_b for div-3 and the initial states of the flip-flop outputs being 1. In this scenario, the XNOR will always output a 1 which leads to a deadlock state as the XNOR output will propagate through the flip-flops. The end result is the MMD output being stuck in 1 until the MC signal is changed.

Taking a closer look on the circuits of Fig. 1, we observe that both circuits consists of two D-flipflops and two NOR-gates. Only the connections differ. The fundamental difference between the connections of the NOR-gates is the polarity and time-instance of the signal. All of these connections can be achieved by introducing a controllable tri-input NOR-gate in place of the common two-input gates.

A. Implementation

The feature set of the original two separate dividers of Fig. 1 can be achieved with a unified more compact design utilizing controllable tri-input NOR gates. The control is used to determine which feedback paths to utilize, which in turn determines the prevalent division ratio.

One significant benefit to using the controllable NOR-gates is the reduction on the number of transistors. If the same operating range is to be achieved with the original two dividers of Fig. 1, an additional multiplexers would be also required for enabling and disabling one of the signal paths. In the proposed merged design, the mode selection does not require additional multiplexers, and is instead provided by the controllable tri-input NOR-gate. The reduction in components naturally leads to a more compact layout.

The final structure of the MMD includes two master-slave type flip-flops and two controllable tri-input NOR-gates. The

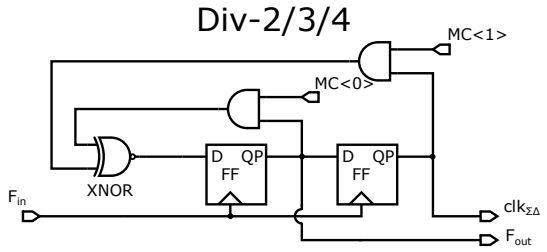

Fig. 4. Prior art div-2/3/4 from [2].

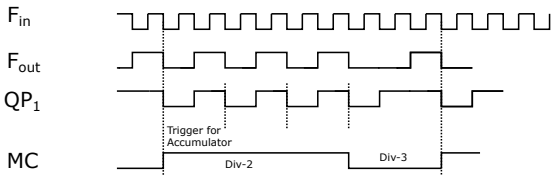

Fig. 5. Timing diagram of the MMD output and the accumulator clock for division by 2.25.

block diagram of the MMD is shown in Fig. 2. The integer division ratio is determined using two individual control bits, the ICW and the MC. ICW is a static control bit and the MC is a dynamic control bit when using fractional division ratios. The dynamic control bit is used as an input to the leftmost NOR-gate, whereas the static ICW sets the proposed design to be logically equivalent to div-2/3 or div-3/4 operation by enabling one of the two controllable inputs of the tri-input NOR-gates. The combination of MC and ICW will determine the division ratio.

The MC is dynamically controlled in the fractional division mode, and thus the proposed design includes an accumulator for counting the pulses for the fractional division ratio. The accumulator is designed using a 13-bit adder together with a 13-bit register. The summation output of the adder is connected to the input of the register, and the output of the register is connected to one of the two inputs of the adder. The adder also has an output for overflow condition. The second input of the adder is connected to a Fractional Control Word (FCW). FCW is a binary representation of the fractional part of N_{frac}. Thus the adder acts on previous residue stored in the register and adds the FCW to it upon the arrival of a trigger signal.

The MC bit is changed whenever the adder overflows. Overflow occurs when summation of the residue stored in the register and the value of the FCW add up to one, which in turn signals the MMD to increment the integer division ratio by one. After the overflow condition is passed, the MC switches back to the original state and the MMD decreases the division ratio. The switching action produces the desired time-average division ratio according to FCW and Eq. 1.

B. Timing

Our proposed design has falling edge triggered flip-flops. In other words, the MMD output changes states during the input signal F_{in} being at the LOW state. This means that

the combinational logic connections can be altered during the LOW state without glitching the output signal. This is due to the use of Master-Slave flip-flops, and the inputs not being active during the LOW state of the F_{in}.

The combinational logic is altered with the accumulator, which means that the trigger from the MMD towards the accumulator has to occur during the F_{in} being LOW. In this case the signal can be taken from QP_1, which is the inverted delayed version of the MMD output. In order to maintain a non-glitching output signal, the effect of the changes in combinational logic have to settle in half the F_{in} period due to the inherent level-sensitivity of the Master-Slave flip-flops. Instantaneous switching is achieved when these two aspects of changing the MC and the settling of the combinational logic in sufficient time are fulfilled. The relationships between the input, output and MC signals in a division by 2.25 is illustrated in Fig. 5.

The combinational logic together with the accumulator loop, will form the bottleneck for performance. The limiting factors for the MMD in terms of input frequency is the delay produced by the critical path. The path consists of the connection between the flip-flops together with the combinational NOR-logic and the accumulator. In the fractional frequency mode, the accumulator is part of the critical path as the MC control loop formed by the MMD and the acumulator.

IV. Simulation Results

The proposed open-loop fractional frequency divider is designed with 28-nm CMOS technology. The layout of the MMD design occupies an area of $40\,\mu\text{m}$ x $30\,\mu\text{m}$ and is depicted in Fig. 6. The robustness and operation of the circuit is confirmed with post-layout simulations with statistical data and process-voltage-temperature sensitivity analysis.

The post-layout simulation results at room temperature of 300 K and typical process corner indicate that the proposed MMD has an operating input frequency range of 0.3–5.4 GHz while consuming DC power of 0.09 – 2.0 mW with a supply voltage of 0.9 V. Extensive Monte-Carlo simulations revealed that the worst process corners are the limiting conditions for the worst operating performance, and therefore the absolute corner simulations define the expected operation region. Process variation sweeps indicate that the slow-slow corner limits the operation the most. The speed reduction limits the frequency range to 0.1–3.6 GHz. On the other hand, the fast-fast corner significantly extends the frequency range to 0.8–8.4 GHz. Frequency range in the extreme slow-fast and fast-slow process corners are closer to the range of the typical corner yielding frequency ranges between 0.3–5 GHz and 0.4–5.8 GHz respectively. Voltage sensitivity wise, the circuit is capable of operating from 0.9 V and above at input frequency of 5.4 GHz, while VDD drop to 0.8 V limits the operation frequency to 4.0 GHz. On the other hand, the circuit tolerates temperature variations very well. Temperature sweeps from 200K–400K and with input frequency of 5.4 GHz resulted in no noticeable effect in the operation. Post-layout time-domain waveforms of the MMD with 5.4 GHz input signal

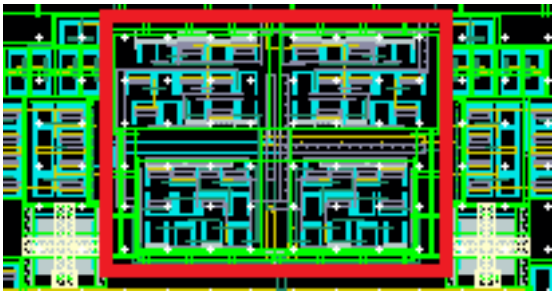

Fig. 6. Layout of the proposed 2/3/4-multimodulus frequency divider. The drawn area is $40\,\mu\text{m}$ x $30\,\mu\text{m}$.

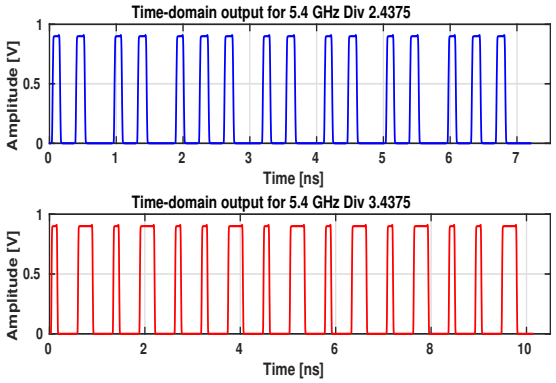

Fig. 7. Post-Layout simulation of 5.4 GHz divided by fractional division ratio of 2.4375 and 3.4375. The time scale is different in the figures.

and division ratios of 2.4375 and 3.4375 are shown in Fig. 7. The figure depicts that the fractional part of the division ratio can be achieved independently of the integer part in time-averaging. In this simulation case, the fractional value can be confirmed to be .4375 by counting the pulses corresponding to div-N and div-(N+1) and observing $X = 9$ and $Y = 7$ for Eq. 1.

V. Conclusion

This paper presents the design and post-layout simulations of a 2/3/4-modulus frequency divider circuit. We have introduced a new circuit structure that combines two logic paths into one, resulting in a compact layout with proper fractional division operation. The proposed MMD design enables operation without forbidden states that could deadlock the synthesized signal.

Our fractional-division based frequency synthesizer generates any output frequency in range of 0.075–2.7 GHz with 0.3–5.4 GHz input signal. The simulation results show that the proposed design consumes on average less than 2 mW when operating at the maximum frequency of 5.4 GHz.

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