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Design and Analysis of an E-band Power Detector in 0.13 µm SiGe BiCMOS Technology

Raju Ahamed[1], Mikko Varonen[2], Dristy Parveg[2], Md Najmussadat[1], Mikko Kantanen[2], Kari A. I. Halonen[1]
[1]Department of Electronics and Nanoengineering, Aalto University, Espoo, Finland
[2]VTT Technical Research Centre of Finland Ltd, Espoo, Finland
Email: raju.ahamed@aalto.fi

***Abstract*—This paper presents a high dynamic range E-band power detector in a 0.13 µm SiGe BiCMOS technology. In this design the Meyer topology using bipolar transistor is adopted and implemented for E-band operation. The measured detector achieves a dynamic range of 35 dB from -25 dBm to +10 dBm. It shows less than 1.6 dB offset in input power detection from 72 GHz to 82 GHz. This power detector consumes 0.6 mW of DC power and the occupied core area is 0.1 mm^2.**

***Index Terms*—BiCMOS, E-band, heterojunction bipolar transistor (HBT), power detector, millimeter-wave, MMIC.**

I. INTRODUCTION

A fully integrated radio frequency (RF) power detector is widely used in many applications including automatic gain control (AGC) and built-in self-test (BIST). BIST enables low cost and time saving testing of internal functionalities of integrated circuits. Power detector is also used to monitor the transmitted power from the transmitter and to control the gain of transmit/receive chain.

There are several methods for power detection such as diode-based, thermal-based and mixer- based. However, not all of them are suitable for implementation. Mixer-based power detectors require an external LO source and large area. Thermal-based detectors can be complicated for on-chip implementation. Diode-based power detectors are widely used for RF signal detection. They are capable of working at very high frequencies [1]. However, in many advanced semiconductor processes high quality schottky diodes are unavailable such as the BiCMOS process used in this work. Meyer [2] developed a power detector utilizing the non-linear rectifying behaviour of the bipolar transistor. The transfer characteristics of Meyer bipolar detector is similar to the diode detectors. This detector has advantages of simplicity, wide bandwidth, low power, small chip size and temperature stability. It can work as a peak detector for large input signal and an rms detector for small input signal [3]. In [3] and [4], they presented power detectors based on Meyer topology. However, maximum operating frequency is limited to 6 GHz in [3] and 20 GHz in [4].

In this paper, an E-band power detector based on the Meyer topology is presented for millimeter-wave applications in a $0.13\,\mu\text{m}$ SiGe BiCMOS process. The effect of matching network in high frequency application on the Meyer power detector has also been analyzed and presented.

II. MILLIMETER-WAVE DETECTOR

A. Circuit Design

The schematic of the Meyer RF power detector is shown in Fig.1. The power detector utilizes two HBTs (M1 and M2) of equal size. Millimeter-wave signal V_{RF} is applied to bipolar transistor M1. The transistor M1 rectifies the applied signal V_{RF}. Transistor M2 generates the DC reference voltage V2 to provide a zero output voltage for zero RF input signal. The output voltage Vo is taken differentially from V1 and V2. Capacitors C1 and C2 are equal valued large capacitors. Their function is to filter out ac signal and power supply noise. The simplified equation for the DC output voltage V_0 in case of large input signal is [2]

$$V_0 = V_{RF} - V_T ln\sqrt{\frac{2\pi V_{RF}}{V_T}} \qquad (1)$$

Where V_{RF} is the peak amplitude of the input RF signal and V_T is the thermal voltage, $\frac{kt}{q}$.

In case of small signal detection, the equation is [3]

$$V_0 = \frac{V_{RF}^2}{V_T} \qquad (2)$$

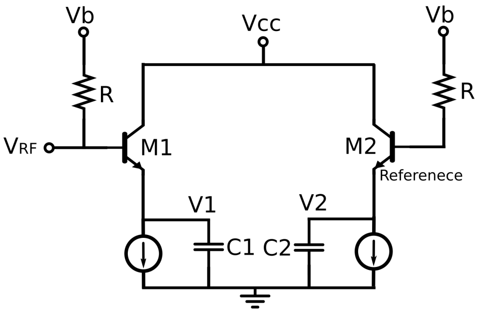

Fig. 1: Schematic of the Meyer RF power detector [2].

Achieving a transistor with input impedance close to 50 Ω is not possible for any number of multiplier in this process. Thus, the input matching network is required to deliver maximum power to the detector. The size of the transistor M1 is chosen in such way that it is easier for impedance matching and the transistor is associated with low parasitic effect. The number of multiplier chosen in this case is 6. Fig.2 shows the designed power detector with input matching elements. The matching network consists of transmission lines and high density MIM capacitors. Input matching in the smith chart is shown in Fig.3 with corresponding point after each element in Fig.2. The transistor input impedance is at point A on the smith chart. A 520 µm biasing line with the RF short capacitor moves the impedance to point B and the DC blocking capacitor moves this impedance to point C. The series transmission line and the shunt line transform this impedance from C to D and D to E, respectively. Finally, the RF pad capacitor moves to point F which is close enough to 50 Ω.

ADS momentum was used for EM simulations of the transmission lines, MIM capacitors and RF pads to obtain accurate modeling. Metal filler exclusion was used for transmission lines, RF pads, transistors and capacitors to prevent the dummy metals. RC extraction of the transistor was performed to take the high frequency parasitic effects into account. A biasing voltage of 0.8 V is applied to both of the HBTs. The current sources are realized by identical current mirrors. The values of filtering capacitor C1 and C2 are 12 pF.

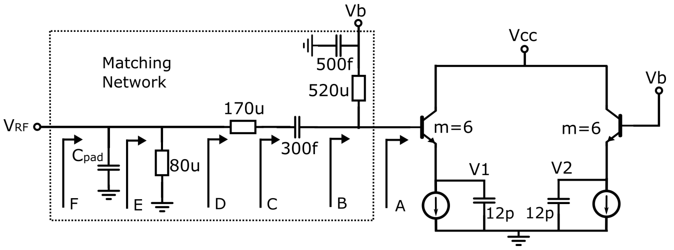

Fig. 2: Implemented power detector with impedance matching elements.

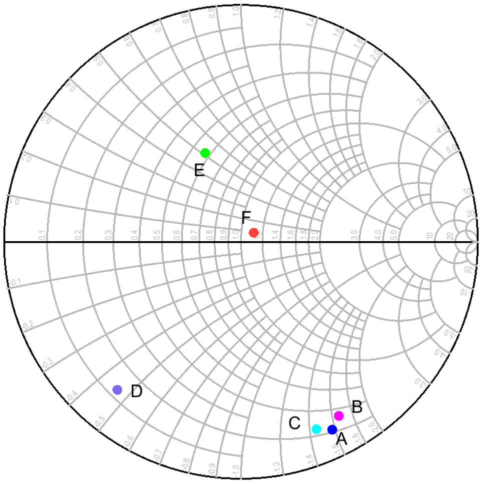

Fig. 3: Input matching of the detector. A, B, C, D, E, F represents corresponding point after each element in Fig.2.

B. Effect of input matching

Input matching network affects the output voltage greatly. Fig.4 shows the simulated voltage responsivity that is defined as the ratio of output voltage and input power in two different cases, with the matching network and without the matching network. It is clear that input matching has a large effect on the responsivity specially for the lower input power. For example, the responsivity with matching network is 25 times higher than the responsivity without matching network at -15 dBm input power. Consequently, it affects the dynamic range of the detector. Without matching network the simulated dynamic range is maximum 15 dB whereas the simulated dynamic range is more than 35 dB with input matching network.

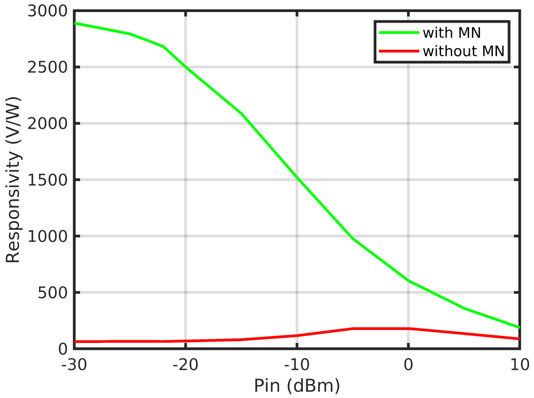

Fig. 4: simulated voltage responsivity of the detector with matching network and without matching network.

III. EXPERIMENTAL RESULTS

The power detector MMIC was fabricated in a 0.13 µm SiGe BiCMOS process. The die micrograph is shown in Fig.5. The core area of the die is 0.1 mm^2.

S-parameters were measured over 30-100 GHz with an Agilent millimeter-wave PNA E8361C network analyzer using 150 µm pitch GSG on-wafer probes and LRRM calibration method. Fig.6 represents the measured and simulated input matching of the MMIC detector. Measured input matching agrees well with the simulation.

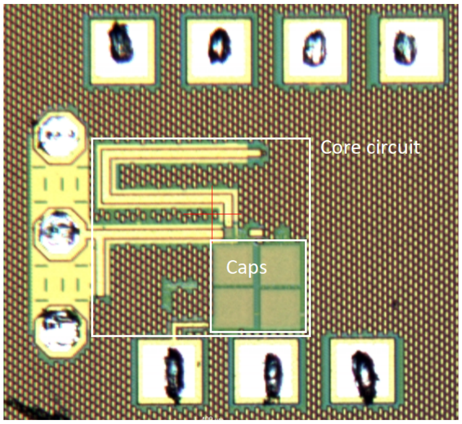

Fig. 5: die micrograph of the power detector.

TABLE I: PERFORMANCE SUMMARY AND COMPARISON TO THE PUBLISHED E-BAND POWER DETECTORS

Ref	Technology	Frequency (GHz)	Dynamic Range (dB)	Area (mm2)	Pdc (mW)
This work	0.13 µm BiCMOS	72-82	35	0.1	0.6
[5]	0.13 µm BiCMOS	58-65	17	-	-
[6]	0.25 µm BiCMOS	75-92	25	-	-
[7]	0.13 µm BiCMOS	71-86	20	-	-
[8]	0.13 µm BiCMOS	65-86	40	0.096	12

Output voltage measurement setup consists of an Agilent signal source, x6 multipliers, digital multimeter, and an Agilent power meter. Agilent E8257D works as a base source and x6 multipliers were used to provide the millimeter-wave input signal. The output voltage was measured differentially between V1 and V2. Fig.7 shows the measured and simulated output voltages while varying the input power at 78 GHz with sinusoidal signal. The results show close agreement between simulations and measurements. The dynamic range of this detector is 35 dB from -25dBm to +10 dBm. Output voltage against input power over different frequencies is plotted in Fig.8. There is less than 1.6 dB variation in input power detection from 72 GHz to 82 GHz.

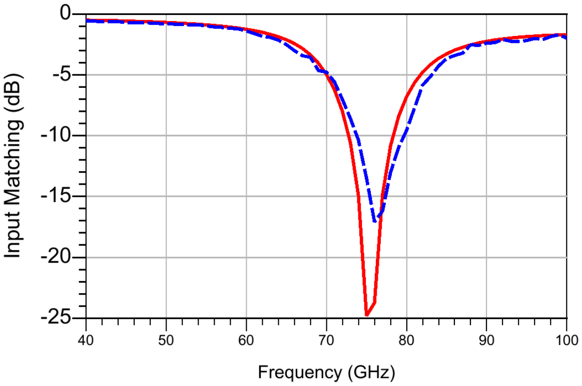

Fig. 6: Simulated (solid) and measured (dashed) input matching of the designed power detector.

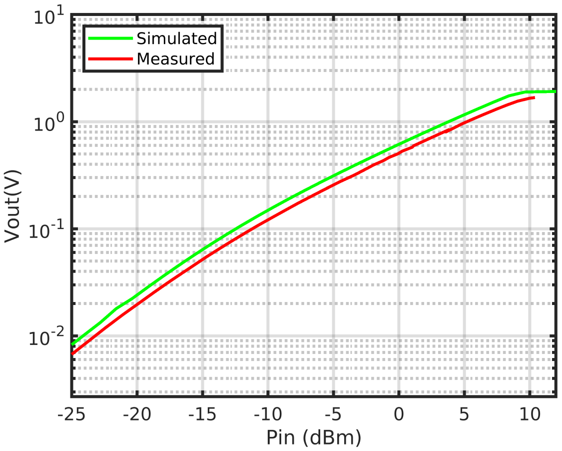

Fig. 7: Simulated and measured output voltage at 78 GHz.

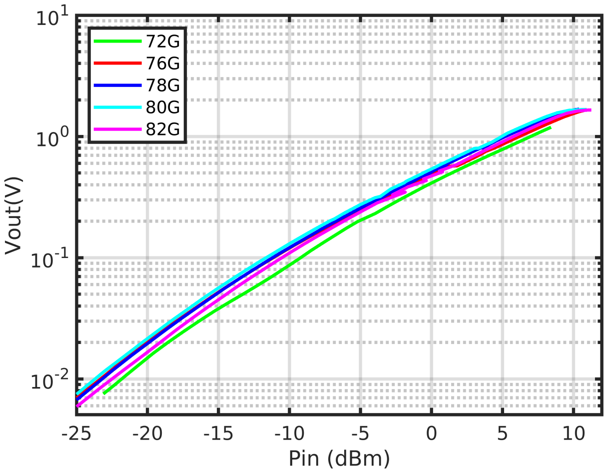

Fig. 8: Measured output voltage over different frequencies.

Table I compares the measured performance of the designed E-band power detector to other published state-of-the-art detectors in SiGe BiCMOS processes. Compared with other works this design presents higher dynamic range with smaller area and low power consumption. Only [8] has 5dB higher dynamic range than this work with similar die area. However, it consumes 12 mW of DC power that is 20 times higher than this work. Considering dynamic range, power consumption and chip area this work shows the best performance at E-band frequencies with BiCMOS technologies.

IV. CONCLUSION

The design and implementation of a low-power and wide-dynamic range E-band power detector has been presented in a 0.13 µm SiGe BiCMOS technology. The results demonstrate that the Meyer detector can be used in E-band utilizing proper input matching network. The measured detector achieved a dynamic range of 35 dB from 72 GHz to 82 GHz with less than 1.6 dB offset in input power over the complete operating frequency range. The power detector consumes 0.6 mW of DC power and the core area is 0.1 mm^2. This detector offers high dynamic range with smaller chip size and low power consumption.

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REFERENCES

[1] R. Han et al., ”280-GHz schottky diode detector in 130-nm digital CMOS,” IEEE Custom Integrated Circuits Conference 2010, San Jose, CA, 2010, pp. 1-4.

[2] R. G. Meyer, ”Low-power monolithic RF peak detector analysis,” in IEEE Journal of Solid-State Circuits, vol. 30, no. 1, pp. 65-67, Jan. 1995.

[3] Tao Zhang, W. R. Eisenstadt and R. M. Fox, ”A novel 5GHz RF power detector,” 2004 IEEE International Symposium on Circuits and Systems (ISCAS), Vancouver, BC, 2004, pp. I-897.

[4] T. Zhang, W. R. Eisenstadt, R. M. Fox and Q. Yin, ”Bipolar Microwave RMS Power Detectors,” in IEEE Journal of Solid-State Circuits, vol. 41, no. 9, pp. 2188-2192, Sept. 2006.

[5] Ullrich R. Pfeiffer and David Goren, ” A 20 dBm Fully-Integrated 60 GHz SiGe Powerm Amplifier With Automatic Level Control”, IEEE J.of Solid-State Circuits, vol. 42, no. 7, July 2007.

[6] R. Malmqvist, C. Samuelsson, D. Dancila, S. Reyaz, M. Kaynak, A.Rydberg, ”Design and test results of a wideband SiGe detector and on-chip slot antenna for W-band sensing applications ”, International Semiconductor Conference (CAS), 2012.

[7] Roee Ben Yishay, Oded Katz, Roi Carmon, Benny Sheinman, Run Levinger, Nadav Mazor and Danny Elad, ”High power SiGe E-band transmitter for broadband communication”, 2013 European Microwave Integrated Circuits Conference (EuMIC).

[8] R. Levinger et al., ”An E-band 40dB dynamic range multi-tanh power detector in 0.13 μm SiGe technology,” 2014 9th European Microwave Integrated Circuit Conference, Rome, 2014, pp. 170-173.