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Operation and Design Consideration of an Ultra High Step-Up DC-DC Converter featuring High Power Density

Hadi Tarzamni, *Student Member*, *IEEE*, Mehran Sabahi, Saeed Rahimpour, Matti Lehtonen, *Member*, *IEEE*, Payman Dehghanian, *Senior Member*, *IEEE*

***Abstract*—A new dual-coupled inductor (CI) single-switch high step-up DC-DC topology featuring high-power density is proposed in this study. Various capacitive power transfer methods, as well as inductive power transfer techniques, are utilized to act as a more efficient power interface between the input and the load. Three ports in the output terminal are employed to distribute the overall output voltage, diminish the voltage ripple in high-voltage gain ratios, and decrease the voltage stress on the port component. In the proposed converter, (i) the voltage gain is high in lower duty cycles of the switching; (ii) the stored energy of magnetizing and leakage inductances are recycled in both CIs; (iii) the switch voltage spikes are alleviated; (iv) the operation is done with no circulating current; (v) low-size passive components are presented; (vi) high-power density is obtained, and the voltage range is widened, and (vii) a simple PWM utilizing a wide control range is provided. In this study, the steady-state operation is analyzed under both continuous conduction mode (CCM) and discontinuous conduction mode (DCM), and the performance of the converter is evaluated using comparisons with similar works. In addition, the experimental results have been provided to justify the feasibility of the design.**

***Index Terms*—DC-DC power conversion, high step-up converter, high power density, coupled inductor.**

I. Introduction

The design of DC-DC converters is typically challenging [1]-[3], where increasing the voltage gain and achieving a higher level of output voltage is always a key concern [4]-[6]. There are some typical approaches that can be utilized to boost the voltage gain, including switched-capacitor (SC) modules, coupled inductors (CIs), and voltage multiplier cells (VMCs). If no inductors are used in the converter structure, switched capacitor converters distribute the voltage stress of the main switch and the capability of the resulting converter in voltage boosting is extendable. Nevertheless, the drawbacks of such converters with low efficiency are the inrush currents of the capacitors during switching transitions, balancing difficulty in the voltage of the capacitors, considerable switching losses, and high current stress over the main switch [7]. In addition, the components suffer from considerably high *di/dt* during their switching transitions. Thus, this issue should be resolved by applying an auxiliary current snubber [8]. Therefore, CIs are still attractive candidates in achieving high voltage gain feature in the DC-DC converters.

Embedding CIs in the converters can be beneficial in increasing the voltage gain, even by setting medium turns ratio of the CI or a medium range of the duty cycle. Doing so will alleviate the issues of reverse-recovery on rectifier diodes. In [9, 10], two similar converters with a single switch and featuring high step-up voltage gain have been presented. These converters combined CI and VMC as an effort to improve voltage gain with recycling the energy in the leakage inductance. The main drawbacks of these converter structures are considerably high inrush current of VMC (within the switching transition time) and higher ripples in the output voltage. Using the same approach, the scholars in [11] utilized two switches in order to achieve a soft-switching performance of the converter. Even though the focus in [11] is on reducing the switching loss, using two switches in the structure leads to the increase in the conduction loss, makes the control of the switches more arduous, and the range of the duty cycle in the main switch will be narrowed. The interleaving method has been utilized in [12] in a coupled-inductor based converter. The presented structure draws current in the input with low ripple, and the voltage stress on the switch has been decreased. On the other hand, the number of semiconductor elements is considerable, where their parasitic capacitances play an important role to ensure faultless operation. The scholars in [13] have combined VMC and CI, and employed them in an interleaved boost converter as an effort to improve the voltage gain in the output terminal of the converter. Nevertheless, the size of the converter is increased due to the use of two large CIs.

Two DC-DC converters with similar structures have been suggested in [14, 15], which employ VMC and CI to reduce the voltage stress while enhancing the voltage gain. However, the leakage inductance and the magnetizing inductance are not suitably applied. A three-phase interleaved converter has been proposed in [16] in order to feature high voltage gain. The structure employs two switches, as well as a coupled inductor in each phase, making the converter bulky and expensive to implement. The DC-DC converter, which is introduced in [17], focused on achieving a high voltage gain and soft-switching performance. The main drawback of this converter is its high input current ripple. In addition, the duty cycle that is needed for achieving the intended voltage gain is high, which yields more conduction loss. Utilizing the interleaved method, two step-up converters have been presented in [18, 19]. These converter structures focused on auto-balancing of the input current. These approaches suffer from some disadvantages, including electromagnetic interference (EMI) problem, considerable resonating currents, and excessive operational modes, which make its control more complex. CI and VMC have been incorporated in [20] to make an interleaved DC-DC converter with high voltage gain and low input current ripple features. Nevertheless, the excessive number of the circuit elements and limited duty cycle range are the main drawbacks of this structure. In the suggested approach in [21], the scholars concentrated on reducing the ripples in the input current. The feasibility of this interleaved-CI DC-DC converter in practical implementation is limited by less efficient VMC.

The state-of-the-art CI-embedded converter topologies are mainly suffering from the following shortcomings: (i) inefficient utilization of leakage and magnetizing inductances, (ii) the issue with the amount of ripples in the output voltage, (iii) excessive utilization of components yielding to lower power density, (iv) circulating current losses, (v) limited duty cycle region, (vi) the issue with the excessive number of CI turns ratio or high duty cycle to achieve high output voltage gains, and (vii) the problem with the inrush current of voltage multiplier cell capacitors during switching transitions. To resolve the abovementioned drawbacks, we propose a high step-up DC-DC converter that mitigates or eliminates the aforementioned limitations with wide applications in electroplating, DC power supplies, motor driving systems, and renewable energy systems such as photovoltaic. The paper is presented in different sections, as operation analytics, calculations of the power loss, design procedure, comparison study and experimental results of a 600W prototype.

II. Proposed Converter

The proposed DC-DC converter utilizing dual-CI and featuring high step-up voltage gain is depicted in Fig. 1. This converter is made up of one power switch (S), six diodes (D_1-D_6), two coupled inductors with two and three windings, and four capacitors (C, C_{o1}, C_{o2}, and C_{o3}). The three-winding coupled inductor is modeled as an ideal transformer with turn ratios of n_1:n_2:n_3, as well as magnetizing inductance (L_m) and leakage inductances (L_{r1} and L_{r2}). The input coupled inductor is also modeled as an ideal transformer with $n_4 : n_5$ turn ratios and inductances of L_n, L_{k1}, and L_{k2}. In the converter structure, the voltage in the input (V_i) is converted to high output voltages (V_{o1}, V_{o2}, and V_{o3}) via flyback and forward techniques. In the output terminal, the configuration of the corresponding capacitors (C_{o1}, C_{o2}, and C_{o3}) provides the output voltage (V_o).

A. CCM Operational Intervals

Continuous conduction mode (CCM) operation of the proposed converter consists of two intervals, which are distinguished by the ON and OFF states of the S switch (Note Fig. 2). The performance of the converter is investigated, assuming the following conditions:

1) The components are considered ideal.
2) The waveforms and the operational analytics are in the steady-state of the converter.
3) The capacitor voltages (V_C, V_{o1}, V_{o2}, and V_{o3}) are assumed to be without any ripple.
4) In case the values of voltage and current are low in the primary (low voltage) and secondary (high voltage) sides of the coupled inductor, respectively, the regarding voltage and current of the leakage inductances (v_{Lr1} and i_{Lr2}) are neglected.

Each operational interval is explained and formulated in the following, and Fig. 3 demonstrates the main components' waveforms in the steady-state of the components assuming the abovementioned conditions. As shown in Fig. 3, the single switch of the proposed converter (S) is driven through a pulse width modulation (PWM) control (G_S), which results in its ON and OFF states in $0<t<DT_S$ and $DT_S<t<T_S$, respectively.

Interval 1 ($0 < t < DT_S$): According to Fig. 2(a), switch S is ON and V_i charges $L = L_n + L_k$ via D_2, which yields:

$$i_L(t) = \frac{V_i}{L}t + I_L(0) \tag{1}$$

where, $I_L(0)$ is the initial current of L at $t = 0$.

The OFF state of D_3 blocks the transfer of the input power to V_{o1}. The stored energy in C charges L_m and is transferred to n_2 and V_{o2} through n_1, which turns the diode D_4 ON. The voltages across L_m and L_{r2} (v_{Lm} and v_{Lr2}) are calculated as

$$v_{Lm} = \frac{V_i}{(1-D)}, \quad v_{Lr2} = V_i \frac{n_2 - D(n_2+n_3)}{n_1(1-D)} \tag{2}$$

where D in the above equation represents the duty cycle of S. Thus, it can be inferred that the sign of v_{Lr2} could be either + or – according to the values of D, n_2 and n_3, which decides the charging or discharging states of L_{r2}—i.e., $di_{Lr2}/dt > 0$ or $di_{Lr2}/dt < 0$. As depicted in Fig. 3, the flow of energy can also be determined in intervals 1 and 2. The following equations outline the operation:

$$\begin{cases} n_2/n_3 > D/(1-D), & L_{r2} \textit{ is charged in } DT_S \\ n_2/n_3 < D/(1-D), & L_{r2} \textit{ is charged in } (1-D)T_S \end{cases} \tag{3}$$

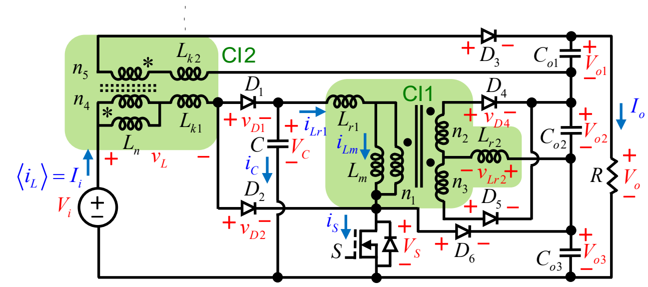
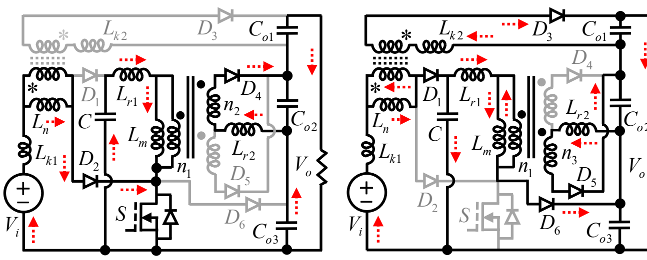


Fig. 1. Proposed structure of high step-up DC-DC converter.



(a) (b)

Fig. 2. Flow of current in Continuous Conduction Mode operational intervals: **(a)** Interval 1. **(b)** Interval 2.

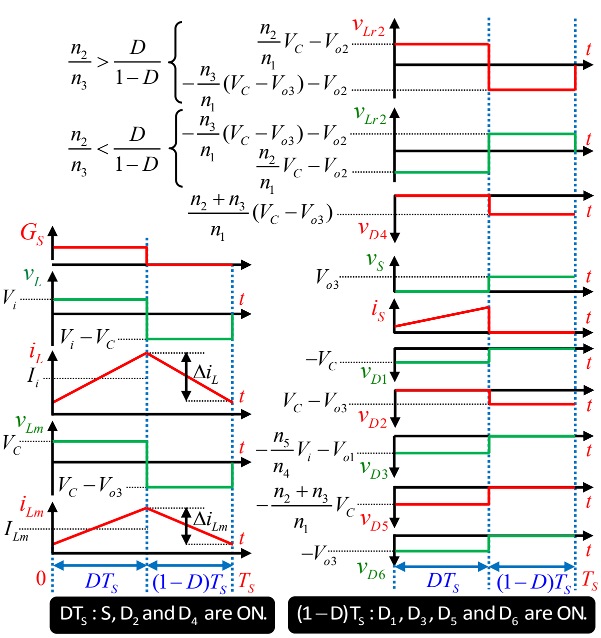


Fig. 3. Main steady-state voltage and current waveforms of Continuous Conduction Mode.

***Interval 2 ($DT_S < t < T_S$)*:** Following the switch duty cycle, S is turned off at $t = DT_S$, which turns the switching states of diodes D_1, D_2, D_3, D_4, D_5, and D_6 into ON, OFF, ON, OFF, ON and ON states, respectively. In the next step, the energy which was saved in the inductance (L_k) is discharged to the capacitor (C). Therefore, that energy is transferred to C_{o3}, where $i_L(t)$ is reduced according to the following equation:

$$i_L(t) = -\frac{V_i D}{L(1-D)}(t - DT_S) + \frac{V_i D}{f_S L} + I_L(0) \tag{4}$$

then, f_s indicates the switching frequency of the converter.

Furthermore, the saved energy in L_n and L_m is discharged to C_{o1} and C_{o2}, respectively, through D_3 and D_5. In case the main switch of the converter is turned OFF, the energy recycle of L_n and L_m in this interval is the same as the flyback converter. Thus, v_{Lm} can be obtained as follows:

$$v_{Lm} = \frac{-V_i D}{(1-D)^2} \tag{5}$$

L_{r2} operates according to the mentioned condition in (3). Hence, v_{Lr2} is calculated by applying (6):

$$v_{Lr2} = V_i \frac{n_3 D - D(1-D)(n_2+n_3)}{n_1(1-D)^2} \tag{6}$$

B. Voltage Gain

The voltage gain of the proposed converter is calculated by applying the volt-second balancing law (VSBL) to the inductors (L, L_m, and L_{r2}), according to the corresponding voltage values in Fig. 3 for the ON period of the switch (DT_S) and the OFF period of the switch ($(1\text{-}D)T_S$). Hence, the voltage gain of each output terminal can be obtained as follows:

$$V_C = \frac{V_i}{(1-D)}, \; V_{o1} = \frac{V_i D}{1-D}\left(\frac{n_5}{n_4}\right) \tag{7}$$

$$V_{o2} = \frac{V_i D}{1-D}\left(\frac{n_2+n_3}{n_1}\right), \; V_{o3} = \frac{V_i}{(1-D)^2} \tag{8}$$

Therefore, the output voltage gain (M) can be derived as follows:

$$M = \frac{V_{o1}+V_{o2}+V_{o3}}{V_i} = \frac{D}{1-D}\left(\frac{n_2+n_3}{n_1} + \frac{n_5}{n_4}\right) + \frac{1}{(1-D)^2} \tag{9}$$

As assessed in (9), M depends on both D and turns ratio of the CIs with direct relation, which provides a large output voltage range. Fig. 4 and Fig. 5 demonstrate two- and three-dimensional graphical views of (9) in terms of D, a, $(n_2+n_3)/n_1$ and n_5/n_4 by assuming a$=n_2/n_1=n_3/n_1=n_5/n_4$.

C. Voltage Stress Analysis

Through the resulted capacitor voltage equations in (7) and (8), the voltage stress of the power switch (S) during $(1\text{-}D)T_S$ can be calculated by applying (10). As depicted in Fig. 6, the normalized form of the voltage stress (V_S / V_o) is with respect to D, a, $(n_2+n_3)/n_1$, and n_5/n_4.

$$V_S = \frac{V_i}{(1-D)^2} \tag{10}$$

According to (10), the voltage stress of the power switch is not dependent on the CIs' turns ratio. Hence, by choosing low-voltage-rated power switches that feature low drain to source resistance as the power switch (S), both conduction loss reduction and high voltage gain with high $(n_2+n_3)/n_1$ and n_5/n_4 values are achievable. The desired operation region from the switch voltage stress viewpoint for design consideration is illustrated in Fig. 7 and Fig. 8 where (i) the higher "a" value, the lower the normalized switch voltage stress, (ii) the most common duty cycle range in high step-up converters ($0.5 < D < 0.85$) has low switch voltage stress, and (iii) the proposed structure for the converter presents an acceptably large switch design area. According to the following equations, the voltage stresses of the diodes can be calculated.

$$|V_{D1}| = \frac{V_i}{(1-D)}, \; |V_{D2}| = \frac{V_i D}{(1-D)^2} \tag{11}$$

$$|V_{D3}| = \frac{V_i}{(1-D)}\left(\frac{n_5}{n_4}\right), |V_{D4}| = \frac{V_i D}{(1-D)^2}\left(\frac{n_2+n_3}{n_1}\right) \tag{12}$$

$$|V_{D5}| = \frac{V_i}{(1-D)}\left(\frac{n_2+n_3}{n_1}\right), \; |V_{D6}| = \frac{V_i}{(1-D)^2} \tag{13}$$

Fig. 9 presents a three-dimensional view of the normalized per unit accumulative voltage stress on diodes to achieve the desired design region for the diodes' voltage in Fig. 10, and Fig. 11. According to these figures, the proposed converter provides an acceptable design area from both "a" and "D" viewpoints. A higher portion of the solution area is allocated to $0.5 < D$, which is more probable in the case of high step-up converters. In addition, increasing $(n_2+n_3)/n_1$ is a better solution than n_5/n_4 to reach high voltage gain by considering the diodes voltage stresses.

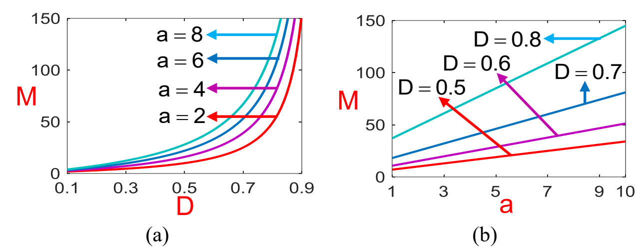


Fig. 4. Voltage gain in terms of; **(a)** Duty cycle. **(b)** CI turns ratio.

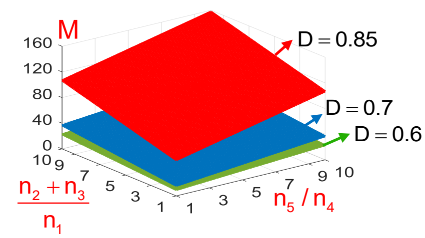


Fig. 5. Voltage gain with respect to $(n_2+n_3)/n_1$ and n_5/n_4.

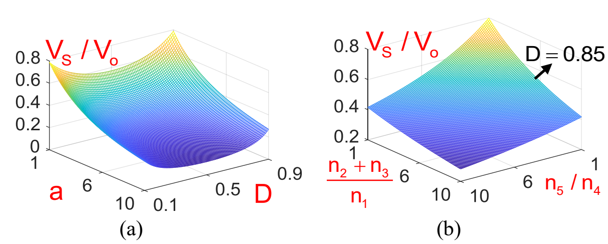


Fig. 6. Normalized switch voltage stress with respect to; **(a)** D and a. **(b)** $(n_2+n_3)/n_1$ and n_5/n_4.

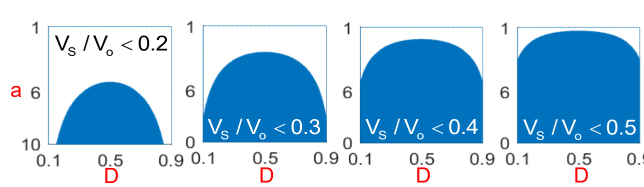


Fig. 7. Desired operation area for low switch voltage stress with respect to a and D.

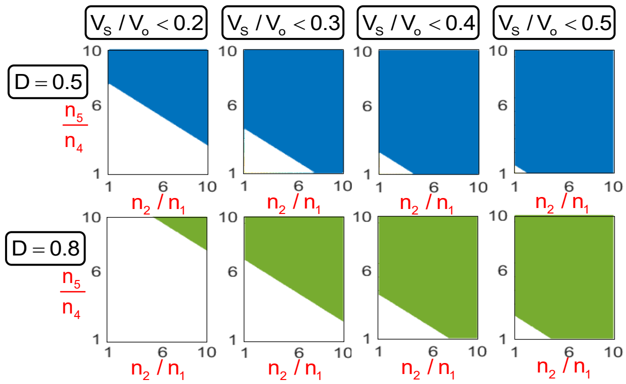


Fig. 8. Desired operation area for low switch voltage stress with respect to $(n_2+n_3)/n_1$ and n_5/n_4 for different D values.

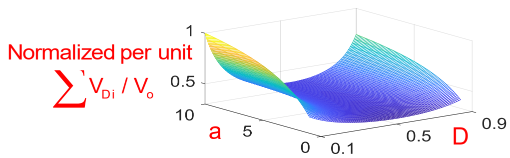


Fig. 9. Normalized per unit accumulative diodes voltage stress.

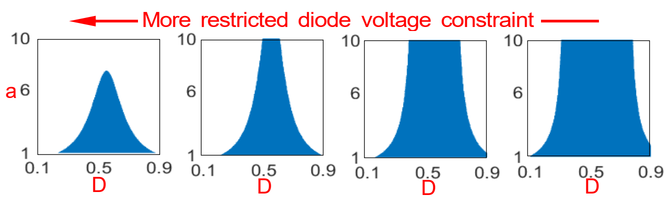


Fig. 10. Desired operation area for diodes' low accumulative voltage stress with respect to a and D.

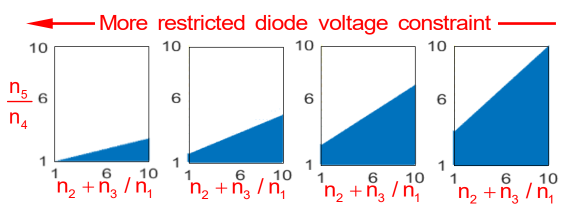


Fig. 11. Desired operation area for diodes' low accumulative voltage stress in D=0.5 with respect to $(n_2+n_3)/n_1$ and n_5/n_4.

D. *Current Stress Analysis*

Fig. 12 demonstrates the steady-state waveforms of i_C, i_{Co1}, i_{Co2} and i_{Co3}, which are derived according to the inductors' average currents. Based on which and through the ampere-second balancing law (ASBL) on the capacitors, the average values of L_{r1} and L_m are obtained as follows:

$$I_{Lr1} = \frac{I_o}{(1-D)} \tag{14}$$

$$I_{Lm} = \frac{n_2 n_3 (1-D) - n_1 n_3 D}{n_1 n_2 (1-D)^2 - n_1 n_3 D(1-D)} I_o \tag{15}$$

where, I_o is the output current equal to V_o/R and R is the output load. Based on (15), I_{Lm} can be either + or – according to the values of D, n_1, n_2, and n_3 (see Fig. 13). In Fig. 13, n_2/n_1 is assumed to be greater than n_2/n_3, considering the converter operating in the high step-up performance mode. Thus, according to equations (14), (15), and considering the path of the current flow (provided in Fig. 2), the current stress of the power switch (S) is obtained as follows:

$$I_S = I_{Lr1} + I_i \tag{16}$$

Likewise, the current stresses of the diodes (D_1 to D_6) in their conducting mode are calculated as follows:

$$I_{D1} = I_{D2} = I_i\,,\ I_{D3} = (n_4/n_5) I_i \tag{17}$$

$$I_{D4} = (n_1/n_2)(I_{Lr1} - I_{Lm})\,,\ I_{D5} = (n_1/n_3) I_{Lm}\,,\ I_{D6} = I_{Lr1} \tag{18}$$

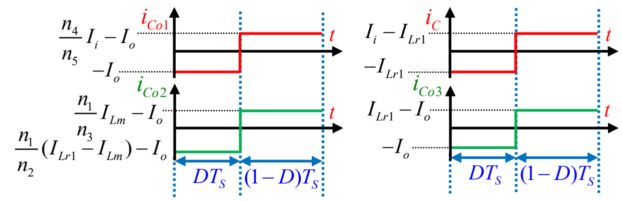


Fig. 12. Waveforms of the capacitors' current according to average value of inductors' current.

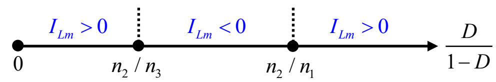


Fig. 13. Identification of magnetizing current sign.

E. *Alleviation in Output Voltage Ripple*

Even though the voltages in the output ports are regulated with an identical degree of freedom (D), V_{o1}, V_{o2}, and V_{o3} do not interact with each other regulation. Hence, the proposed triple-output port converter can be adjusted in an optimal operation zone by setting D, n_2/n_1, and n_3/n_1 to alleviate the amount of the overall output voltage ripple (Δv_o). Employing the current waveforms in Fig. 12, the schematic of the voltage ripple from each port (Δv_{o1}, Δv_{o2}, and Δv_{o3}) is demonstrated in Fig. 14. Considering Fig. 12 and $dv_C/dt = i_C/C$, it can be inferred that dv_{o1}/dt and dv_{o3}/dt are negative and positive in DT_S and $(1\text{-}D)T_S$, respectively. Nevertheless, charging or discharging state of V_{o2} is conditional on the values of D, n_2/n_1, and n_3/n_1. Hence, the reverse sign of dv_{o2}/dt compared to dv_{o1}/dt and dv_{o3}/dt results in the reduced Δv_o by $|\Delta v_{o1}+\Delta v_{o3}-\Delta v_{o2}|$. In Figs. 14(a) and (b), the slopes of $V_{o1}(V_{o3})$ and V_{o2} have identical and different signs, respectively. Subsequently, Fig. 14(b) presents a better condition. The output voltage can be reduced if the following condition is satisfied:

$$\frac{n_2(1-D) - n_1 D}{n_2(1-D)^2 - n_3 D(1-D)} < 1 \tag{19}$$

Accordingly, the operation zone of the alleviated Δv_o is depicted in Figs. 15 and 16. The operation zone in Fig. 15 is demonstrated with respect to n_2/n_1 and n_3/n_1 with different values of D. As demonstrated in Fig. 15, the colored area shows the alleviated Δv_o. One can see that the higher the n_2/n_1 and n_3/n_1 in the desired region, the higher the V_o, the lower the Δv_o, and accordingly, considerably lower ratio of output voltage ripple to the output voltage ($\Delta v_o/\ V_o$) will result. Likewise, the intended zone is demonstrated in Fig. 16 in terms of n_2/n_1 and D. This zone includes a considerable part of the likely operation zone. It's clear that the intended zone is wider with a higher D in Fig. 15 and larger n_3 to n_1 ratio, according to Fig. 16. The small output voltage ripple feature of the proposed structure makes the converter an interesting option for some industrial applications like electroplating.

F. *Input Current Ripple*

Considering the operational analytics presented in Section II Part A, the normalized input current ripple is equal to

$$\frac{\Delta i_L}{I_i} = \frac{DR}{f_S L M^2} \tag{20}$$

According to the above equation, the desired operation region for the input CI to reach a specific input current ripple is expressed in Fig. 17. In this figure, higher "D" and "a" correspond to lower normalized input current ripple, which leads to small CI size for a certain L, and accordingly, high power density.

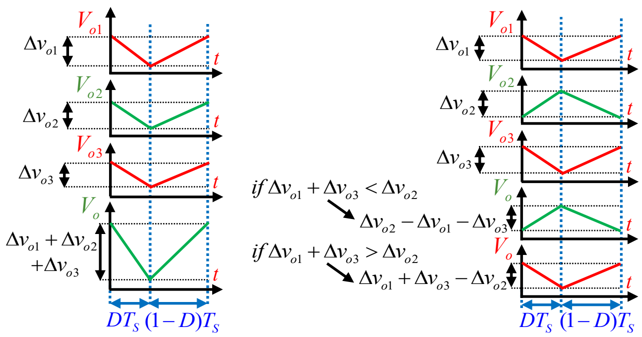


Fig. 14. Output voltage ripple;**(a)** Additional. **(b)** Subtractive (desired).

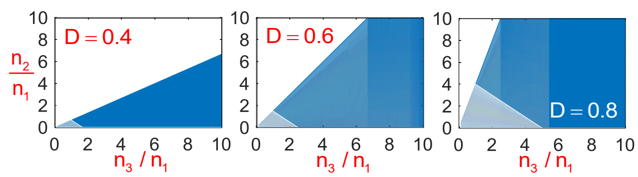


Fig. 15. Operation zone for the output voltage ripple alleviation according to n_2 to n_1 ratio and n_3 to n_1 ratio.

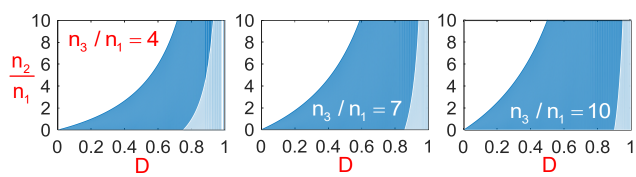


Fig. 16. Operation zone for the output voltage ripple alleviation in terms of n_2/n_1 and D.

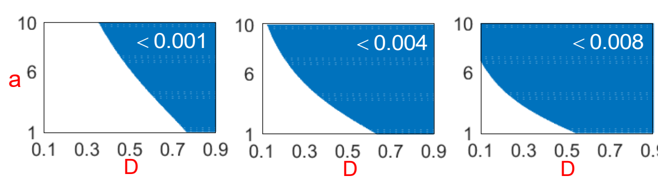


Fig. 17. Desired operation zone of input CI for different $\Delta i_L f_s L / R\, I_i$ limitations with respect to a and D.

G. DCM-CCM Boundary

According to (9) and the boundary conduction mode average input current (I_{iB} = Δi_L /2), the average output current and load resistance in boundary conduction mode can be obtained as follows:

$$I_{oB} = \frac{DV_o}{2f_S LM^2}\ ,\ R_B = \frac{2f_S LM^2}{D} \tag{21}$$

According to (21), the operation zone of CCM can be recognized on the normalized output current in Fig. 18(a) and (c). In addition, the operation zone in discontinuous conduction mode (DCM) is depicted in load resistance planes in Fig. 18(b) and 18(d). According to Fig. 18, it can be inferred that increasing "a" yields a wider solution region in continuous conduction mode for the normalized output current. As "a" becomes larger in discontinuous conduction mode, the solution space widens for load resistance.

H. DCM Operation

Since the proposed converter structure utilizes two coupled inductors, various discontinuous conduction mode conditions can be introduced. As two mostly likely DCM conditions, discontinuous currents of only L_r, and both L_k and L_r are considered in this paper, which yield DCM and extremely discontinuous conduction mode (EDCM), respectively. In Fig. 19, the voltages of the inductors in discontinuous conduction mode and extremely discontinuous conduction mode are demonstrated. According to Fig. 19 and the VSBL, the voltage gains in DCM and EDCM can be obtained as follows:

$$M_{DCM} = \frac{D_1}{D_1+D_2}\left(\frac{n_2 - n_2D_1 + n_3D_2}{n_1(1-D_1)^2}\right) + \frac{n_5D_1}{n_4D_2} + \frac{1}{(1-D_1)^2} \tag{22}$$

$$M_{EDCM} = \frac{(1-D_4)}{(D_2+D_3)}\left(\frac{D_1}{n_1(D_1+D_2)}\left(n_2 + \frac{n_3D_2}{1-D_1}\right) + \frac{1}{1-D_1}\right) + \frac{n_5D_1}{n_4D_2} \tag{23}$$

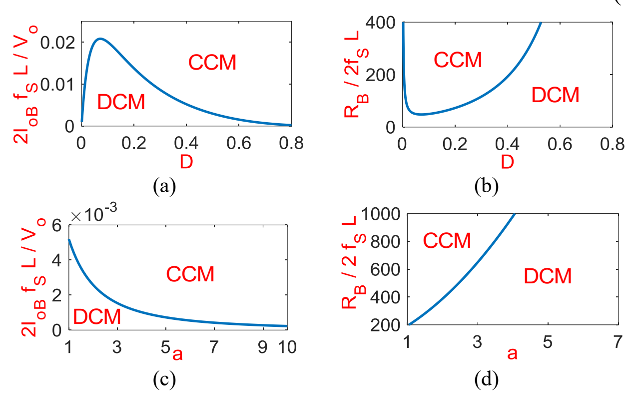


Fig. 18. BCM operational characteristics; **(a, b)** Normalized output current and normalized load resistance in a = 3. **(c, d)** Normalized output current and normalized load resistance in D = 0.6.

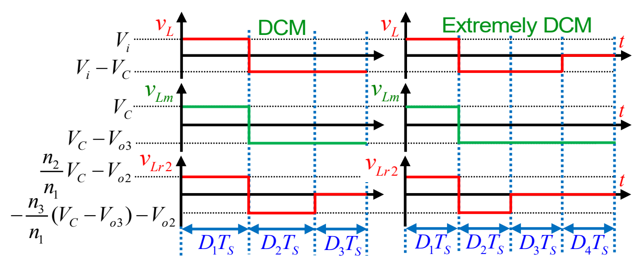


Fig. 19. Waveforms of Inductors' voltage in two key discontinuous conduction operation modes.

I. Efficient Inductive Utilization

The recycling of the stored energy in the passive components of the circuit and transferring it to the load have been accomplished by utilizing various capacitive and inductive methods. These methods were meant to avoid the circulating current. The inductors' discharge paths to the output load is demonstrated in Fig. 20. According to Fig. 20, the proposed converter structure (i) provides a path to guide the stored energy of C to C_{o2} via n_1 and n_2 utilizing a forward method during DT_S, (ii) saves the stored magnetizing energy of L_n and L_m to C_{o1} and C_{o2}, respectively, utilizing a flyback method during (1-D)T_S, and (iii) reprocesses the harvested energy of L_{k1}, L_{r2}, and L_{r1} toward C, C_{o2} and C_{o3}, respectively. Note that, these energy flow paths are corresponded to their numbers in Fig. 20. Since the energy of all parasitic inductances (including leakage and magnetizing) is recycled, there is no need for an accurate design feature for the coupled inductors to realize the intended operation. Hence, a basic and simple coupled inductor can also be employed in the proposed structure.

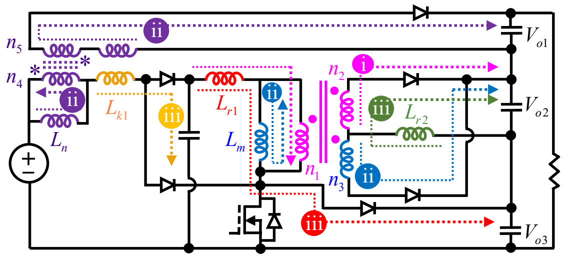


Fig. 20. Graphical paths of inductive power flow in proposed converter solution.

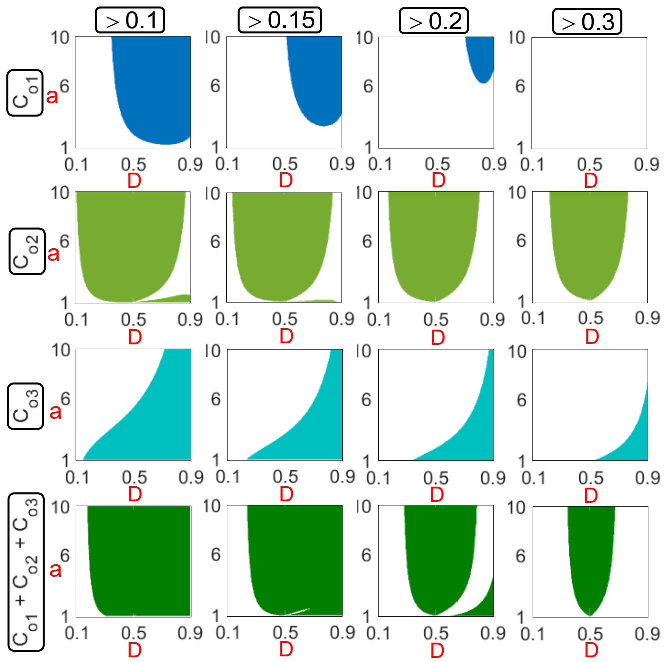


Fig. 21. Desired operation region for high energy transfer of output capacitors with different $\Delta w_C f_s R / V_o^2$ limitations.

J. Energy Analysis

Using the following equations, the exchanged energy of each passive element during one switching period ($1/f_s$) can be calculated.

$$\Delta w_L = \frac{M^2 V_i^2 D}{Rf_S}, \quad \Delta w_{Lr} = \frac{DMV_i^2(n_2 - D(n_2+n_3))}{n_1 R f_S (1-D)^2} \tag{24}$$

$$\Delta w_{Lm} = \frac{MV_i^2 D(n_2 n_3 (1-D) - n_1 n_3 D)}{Rf_S(n_1 n_2 (1-D)^3 - n_1 n_3 D(1-D)^2)} \tag{25}$$

$$\Delta w_{Co1} = \frac{MV_i^2 D^2 n_5}{Rf_S(1-D)n_4}, \quad \Delta w_{Co3} = \Delta w_C = \frac{MV_i^2 D}{Rf_S(1-D)^2} \tag{26}$$

$$\Delta w_{Co2} = \frac{MV_i^2 D(n_2+n_3)}{Rf_S n_1(1-D)}\left(\frac{n_2(1-D)-n_1 D}{n_2(1-D)-n_3 D} - 1 + D\right) \tag{27}$$

Equations (26) and (27) lead to Fig. 21, which demonstrates the desired operation region of the proposed converter to obtain high energy transfer in the output capacitors with different $\Delta w_C f_s R/V_o^2$ limitations. This figure presents the energy characteristics of the output capacitors in each row, which results in the overall feature in the last row. Moreover, the limitation becomes more restricted from left to right. According to Fig. 21, (i) C_{o1} and C_{o2} transfer the lowest and the highest energy in the same operational condition, (ii) $0.5 < D$ and higher "a" have higher energy transfer, and (iii) the proposed converter presents high energy transfer (power density) in most of its common operation region at the output terminal.

III. Power Loss Assessment

The model, which is depicted in Fig. 22, demonstrates the components of the proposed converter, including their real circuit representations. In this practical model, (i) internal resistance are considered in series with the passive components, (ii) the diodes are represented with their forward voltage drop (V_F) and series resistance (r_D), and (iii) a drain-source ON resistance (r_S) models the conduction loss and also a parasitic capacitance (C_S) model indicates the switching losses of the switch S. Besides, the coefficients of hysteresis and eddy current loss (C_{Hys} and C_{Eddy}), core effective cross-sectional area (A_{CI1} and A_{CI2}) of the coupled inductors, and effective core volume (U_{CI1} and U_{CI2}) of the coupled inductors are the empiric parameters in calculating the value of the core loss [22]. As stated by the steady-state analysis, the power loss equations of the components are summarized in Table I.

TABLE I. Power Loss Equations of Components.

Component	Power Loss Equation
S (Conduction Loss)	$P_S^{Cond} = \frac{r_S P_o D}{R}\left(\frac{1}{1-D}+M\right)^2$
S (Switching Loss)	$P_S^{Sw} = \frac{f_S C_S P_o R}{2M^2(1-D)^4}$
D_1	$P_{D1} = \frac{r_{D1} P_o M^2(1-D)}{R} + V_F M(1-D)\sqrt{\frac{P_o}{R}}$
D_2	$P_{D2} = \frac{r_{D2} P_o M^2 D}{R} + V_F MD\sqrt{\frac{P_o}{R}}$
D_3	$P_{D3} = \frac{r_{D3} n_4^2 P_o M^2(1-D)}{n_5^2 R} + V_F M(1-D)\frac{n_4}{n_5}\sqrt{\frac{P_o}{R}}$
D_4	$P_{D4} = \frac{r_{D4} D n_1^2}{n_2^2}(I_{Lr1}-I_{Lm})^2 + \frac{V_F D n_1}{n_2}(I_{Lr1}-I_{Lm})$
D_5	$P_{D5} = \frac{r_{D5} n_1^2 I_{Lm}^2(1-D)}{n_3^2} + \frac{V_F I_{Lm} n_1(1-D)}{n_2}$
D_6	$P_{D6} = \frac{r_{D6} P_o}{R(1-D)} + V_F\sqrt{\frac{P_o}{R}}$
L_k and L_{r1} (Winding Loss)	$P_{Lk}^W = \frac{r_{Lk} M^2 P_o}{R}, \quad P_{Lr1}^W = \frac{r_{Lr} P_o}{R(1-D)^2}$
CI_1 Hysteresis Loss	$P_{CI1}^{Hys} = \frac{C_{Hys} V_i^2 D^2 U_{CI1}}{4(1-D)^2 n_1^2 f_S A_{CI1}^2}$
CI_2 Hysteresis Loss	$P_{CI2}^{Hys} = \frac{C_{Hys} V_i^2 D^2 U_{CI2}}{4N^2 f_S A_{CI2}^2}$
CIs Eddy Current Loss	$P_{CI1}^{Eddy} = \frac{C_{Eddy} V_i^2 D U_{CI1}}{N^2 A_{CI1}^2 (1-D)^3}, \quad P_{CI2}^{Eddy} = \frac{C_{Eddy} V_i^2 D U_{CI2}}{N^2 A_{CI2}^2 (1-D)},$
C	$P_C = \frac{r_C P_o}{R}\left(\frac{D}{(1-D)^2} + (1-D)(M - \frac{1}{1-D})^2\right)$
C_{o1}	$P_{Co1} = \frac{r_{Co1} P_o (1-D)}{RD}\left(\frac{n_2(1-D)-n_1 D}{n_2(1-D)^2 - n_3 D(1-D)} - 1\right)^2$
C_{o2}	$P_{Co2} = \frac{r_{Co2} P_o D}{R(1-D)}$

IV. Non-Ideal Converter Voltage Gain

According to the ideal converter voltage gain in (9) and the power loss calculations in Section III, the voltage gain of the converter in non-ideal condition (M') can be obtained as follows:

$$M' = \frac{M}{1+(P_{Loss}/P_o)} \tag{28}$$

where P_{Loss} is the total power loss. Fig. 23 depicts a comparison of M and M' with respect to "D" and "a".

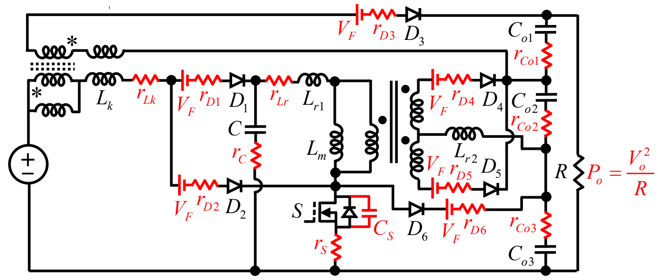


Fig. 22. Real (non-ideal) model of the components of the proposed converter.

V. Design Procedure of Passive Components

The design of the passive circuit elements of the proposed converter can be accomplished using the equations (29)-(33) as follows:

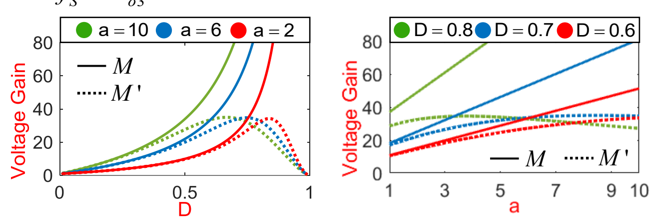
$$L_n = \frac{DV_i}{f_S \Delta i_L} \tag{29}$$

$$L_m = \frac{DV_i}{f_S \Delta i_{Lm}(1-D)}, \quad L_{r2} = \frac{n_2 DV_i(n_2 - D(n_2+n_3))}{n_1^2 f_S \Delta i_{Lr1}(1-D)} \tag{30}$$

$$C = \frac{DV_o}{f_S R \Delta v_C (1-D)}, \quad C_{o1} = \frac{DV_o}{f_S R \Delta v_{Co1}} \tag{31}$$

$$C_{o2} = \frac{V_o}{R f_S \Delta v_{o2}}\left(\frac{n_2(1-D)-n_1 D}{n_2(1-D)-n_3 D} - 1 + D\right) \tag{32}$$

$$C_{o3} = \frac{DV_o}{f_S R \Delta v_{o3}} \tag{33}$$



(a) (b)

Fig. 23. Ideal and non-deal voltage gain comparison with respect to: **(a)** Duty cycle. **(b)** CI turns ratio.

VI. Comparisons

The converter design cannot fulfill all goals and may have some weak points, as well as realizing the power points. In this section, a comparison is made in the design and performance metrics corresponding to the proposed approach against other step-up DC-DC structures, which are based on the coupled inductor and have recently been introduced. A numerical comparison is made available in Table II with respect to the number of components (*#S*, *#D*, *#L/CI* and *#C*) and VMC utilization. According to Table II, topologies in [10], [23], [24], [30], [31] and the proposed structure possess the least achievable number of switches. Less switch yields less number of gate drivers, which also reduces the cost. Besides, in the proposed structure, a reasonable number of semiconductors have been employed, considering the utilization of three output terminals to harvest all passive components' energy. The presented structures in [16], [18], and [20] have the highest number of passive elements, leading to higher weight and size of the converter. Meanwhile, the number of employed passive components is acceptable in the proposed converter considering its generated output voltage level. In addition, the proposed structure operates without any voltage multiplier cells, which results in no capacitive inrush currents during the switching transitions of voltage multiplier cell. The performance of voltage and energy are compared in Fig. 24. According to Figs. 24(a) and (b), the proposed approach achieves the highest voltage gain in comparison with similar works with respect to the duty cycle and turn ratio of the coupled inductor as the main duty. From the inductive point of view, the value of normalized Δw_L in the proposed structure is the highest in Figs. 24(c) and (d). According to Figs. 24(c) and (d) and considering the fact that a normalized form has been chosen for comparison, it can be inferred that (i) the proposed converter utilizes the lowest-size inductor in its input in a certain V_i, Δi_L and f_s, (ii) the amount of power density in the proposed DC-DC converter is the highest, and (iii) the proposed converter is applicable in renewable energy applications due to its features. In order to provide a comprehensive evaluation, a cost function (*CF*) is defined as follows:

$$\begin{aligned} CF = &+x_1\hat{M} - x_2\Delta\hat{i}_L + x_3\Delta\hat{w}_L - x_4\sum\hat{V}_S - x_5\sum\hat{V}_D \\ &- x_6\hat{N}_S - x_7\hat{N}_D - x_8\hat{N}_L - x_9\hat{N}_C - x_{10}\hat{N}_{OM} - x_{11}V\hat{M}C \end{aligned} \tag{34}$$

where, $\hat{M}$, $\Delta\hat{i}_L$, $\Delta\hat{w}_L$, $\sum\hat{V}_S$ and $\sum\hat{V}_D$ are the normalized voltage gain, input current ripple, input energy, and accumulative switch and diode voltage stresses, respectively. $\hat{N}_S$, $\hat{N}_D$, $\hat{N}_L$, $\hat{N}_C$ and $\hat{N}_{OM}$ are the normalized number of utilized switches, diodes, inductors, capacitors and operational modes, respectively, in each converter. Note that, each aforementioned factor is normalized with the highest value of that parameter among converters, which leads them to the values of "≤ 1". Furthermore, $V\hat{M}C$ is equal to "1" or "0" for the converters with or without voltage multiplier cells, and x_i are the weight coefficients which are assumed as $x_i = 1$ in this paper. In (34), the features and drawbacks are presented with "+" and "$-$" signs, respectively. According to the definitions, higher *CF* results in better converter characteristics from the generalized point of view, which is assessed in Fig. 24(e). Based on the highest *CF* value of the proposed converter in Fig. 24(e), it can be deduced that the proposed converter expresses notable promising advantages with an economical, high power density, ultra-high voltage gain, low-volume, uncomplicatedly-controlled, and efficient topology.

TABLE II. General Comparison of the Proposed Converter with Other Newly-introduced Converters based on Coupled Inductors. (**Pro:** Proposed)

Ref.	Pro	[10]	[11]	[12]	[13]	[14]	[15]	[16]	[17]
#S	1	1	2	4	2	2	2	6	2
#D	6	4	2	4	4	4	4	4	2
#L+CI	0+2	0+1	1+1	2+1	0+2	0+1	0+1	0+3	0+1
#C	4	4	4	3	3	5	5	7	5
#VMC	×	✓	✓	×	✓	✓	✓	✓	×
Ref.	**[18]**	**[19]**	**[20]**	**[23]**	**[24]**	**[26]**	**[27]**	**[30]**	**[31]**
#S	4	4	2	1	1	4	2	1	1
#D	6	2	6	4	4	0	2	4	5
#L+CI	2+2	0+2	0+2	0+1	0+1	0+1	1+1	0+1	0+1
#C	9	3	5	4	4	3	4	4	5
#VMC	✓	✓	✓	✓	✓	✓	✓	✓	✓

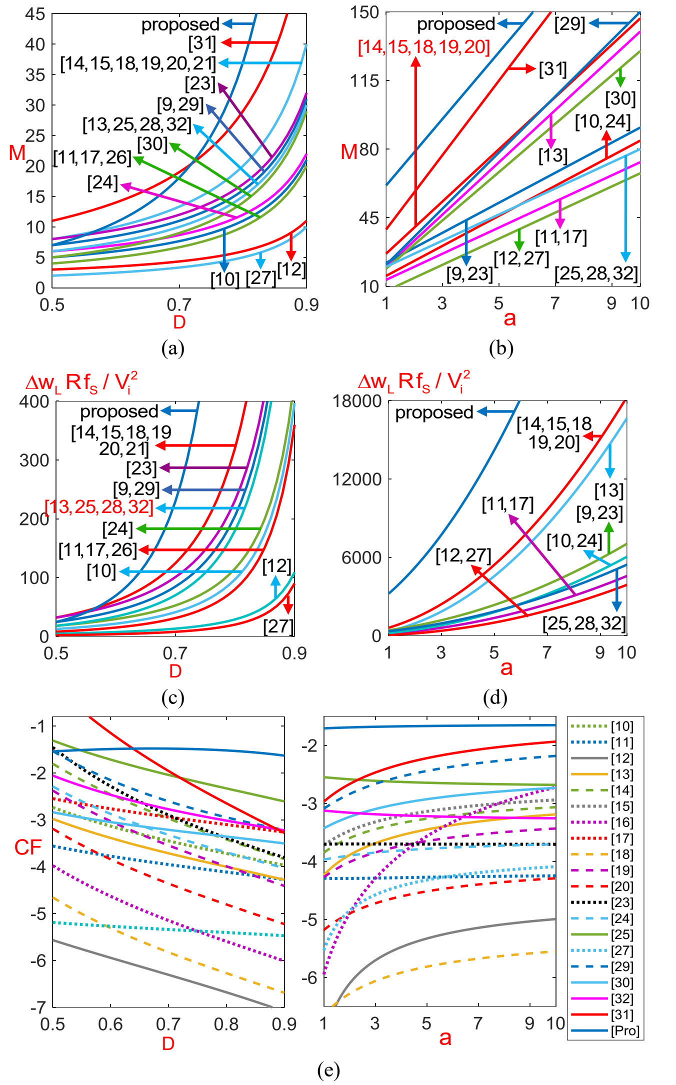


Fig. 24. Comparison of the CI-based DC-DC converters' performances in CI turn ratio of 1 and D=0.85; **(a, b)** Output voltage gain. **(c, d)** Normalized transferred energy of the input CI in one switching cycle. (e) Generalized cost function.

VII. Experimental Validation

A 600 W prototype with the power density of 1.028 W/cm^3 has been provided to validate the theoretical analytics of the proposed approach. For the circuit elements, IRFP4868pbf, HER3003PT, and HER3006PT are selected as the switch and diodes, respectively. One 33 µF, one 22 µF, and two 6.8 µF electrolyte capacitors are chosen for C, C_{o1}, C_{o2}, and C_{o3}, respectively, to limit the voltage ripple by 2% in V_C, V_{Co1}, V_{Co2} and V_{Co3} based on (31) and (32). Moreover, n_1=8, n_2=16, n_3=16, n_4=15, and n_5=30 are designed for the CIs with EE55 cores, respectively. The control of the proposed converter implemented by the LPC1768 ARM microcontroller.

In the experiment, the input voltage and power of the proposed converter are $V_i = 24$ V and $P_{in} = 416$ W, respectively. In addition, the switching frequency is $f_s = 50$ kHz. The results of the test are depicted in Fig. 25. According to Fig. 25(a), the applied gate pulse of the power switch S is D = 0.6 which results in the switch current curve with I_S = 20A. In this duty cycle, v_L is demonstrated in Fig. 25(b). v_L in the experimental results confirms the theoretical charge ($v_L \approx$ 24V) and discharge ($v_L \approx$ -36V) values in DT_S and (1-D)T_S, respectively. The voltage waveforms of the semiconductors are depicted in Figs. 25(c)-(i), where the approximate voltage stresses of $V_S \approx$ 150V, $V_{D1} \approx$ 60V, $V_{D2} \approx$ 90V, $V_{D3} \approx$ 120V, $V_{D4} \approx$ 360V, $V_{D5} \approx$ 240V and $V_{D6} \approx$ 150V are observed, validating (10)-(13), respectively. The proposed converter expresses low-voltage spikes during the switching transitions. Hence, the proposed structure is a good choice in the applications where high voltage and high frequency are required. Figs. 25(j)-(l) demonstrate the voltages across C, C_{o1}, C_{o2}, and C_{o3}, where the experimental results of V_C=58V, V_{Co1}=70V, V_{Co2}=140V and V_{Co3}=147V nearly realize V_C=60V, V_{Co1}=72V, V_{Co2}=144V and V_{Co3}=150V as the theoretical results. As depicted in Fig. 15, the converter's operation point is located in the desired Δv_o reduction region that satisfies Fig. 14(b). The discontinuous conduction mode is also applied to the prototype, and v_L is demonstrated in Fig. 25(m), which validates the theoretical analytics in Fig. 19. Finally, the load step change effect on the output voltage is evaluated in Fig. 25(n), where the load value is increased. Eventually, the converter prototype and the efficiency plots comparison are provided in Fig. 26, which verifies the acceptable efficiency of the proposed topology.

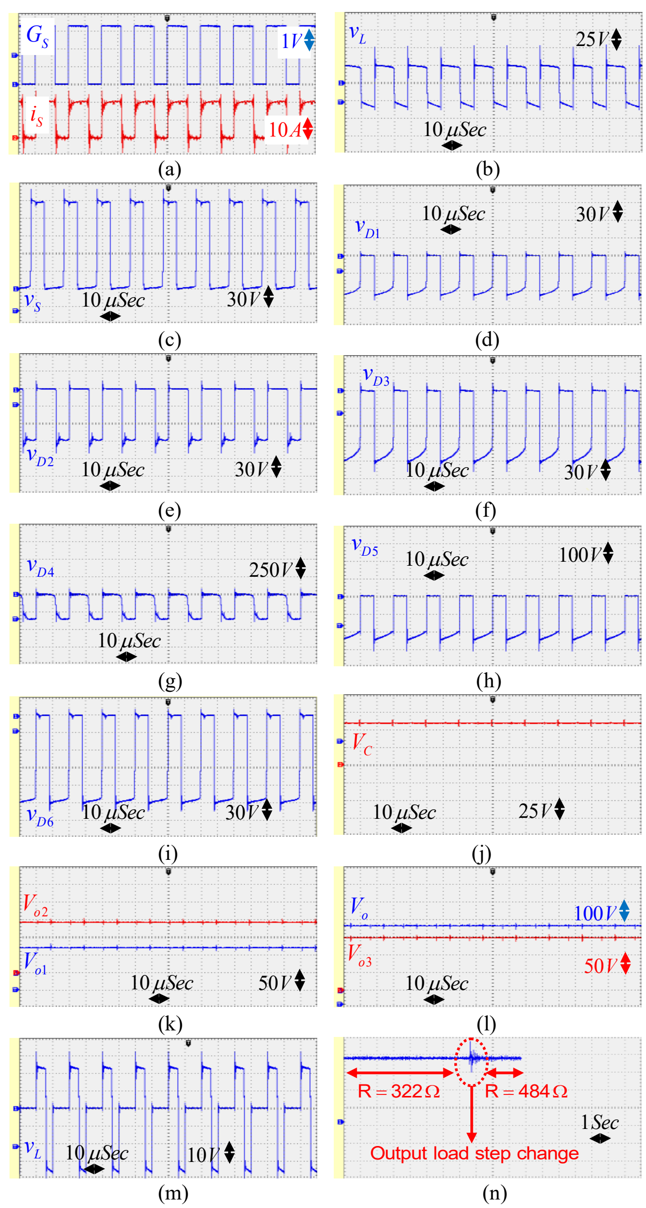
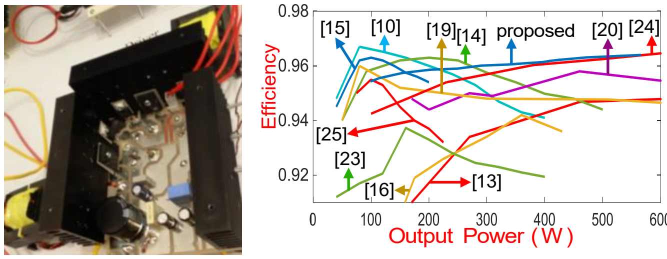


Fig. 25. Experimental results.



(a) (b)

Fig. 26. (a) Prototype. **(b)** Converter efficiency with respect to the output power.

VIII. CONCLUSION

A state-of-the-art high step-up DC-DC converter has been proposed in this study. The proposed structure has been analyzed and validated via a 600 W experimental prototype. It has several key characteristics, including (i) employing different inductive and capacitive methods to transfer the input power and harvested magnetic energy to the output load, (ii) achieving a high voltage gain with lower turns ratio in the coupled inductor, and (iii) utilizing a simple PWM control with an extensive duty cycle range. The major properties of the proposed approach were thoroughly investigated and numerically compared with those of the state-of-the-art architectures. Detailed design discussion is provided to achieve the desired operational region regarding the semiconductors' voltage stress reduction, power density improvement, and ripple reduction in the input current and output voltage to make them smoother. A 600W prototype has also been provided to validate the theoretical analyses. The experimental results confirm the voltage gain of 14.8 and an appropriate efficiency range of 94.7% - 95.8%.

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