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# Efficiency of a Voltage Sourced Inverter with Controllable Intermediate DC Voltage

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## Keywords

AC machines, Adjustable speed drives, Variable speed drives, Efficiency, Induction motors.

## Abstract

The efficiency of a low cost three-phase PWM (Pulse-Width-Modulated) VSI (Voltage Source Inverter) is evaluated in this paper based on the fact that a controllable DC-link is available. The study was conducted considering that a VSI should supply a three-phase low-voltage induction motor, with rated power of 500 kW supplied with a industrial voltage of 690 V. Results presented in this paper are based on computer simulations and analytical expressions for calculation of losses. The goal is to improve the overall efficiency on the inverter part of the ASD (Adjustable-Speed-Drive), especially at low speed region without harming the current and torque quality, which should be kept within acceptable values.

The circuit topology is a conventional two level IGBT-based three-phase voltage source inverter. A two-level natural sampling PWM with sine-wave modulation was used in order to generate the control pulses for the IGBT's and hence allowing the output voltage level to be varied. Scalar control of the inverter output voltage was implemented in order to allow the maximum air gap flux in the motor. Using an ideal (without ripple) and controllable intermediate DC-link voltage stage, several computer simulations are accomplished and waveforms are used to evaluate the inverter performance. The objective of the so-called open-loop simulations is to verify how the circuit behaves and to have a simple indication on trend of the results.

The final results clearly show that by lowering the DC-link voltage, the switching losses of the inverter can be reduced, especially at low speeds. Also torque quality and total harmonic distortion of the output current are slightly improved.

## Introduction

This paper deals with the efficiency of a voltage source inverter stage when different values of the DC-link voltage are used. Efficiency is directly related with losses of the components in use, which by its turn is strongly dependent on their internal physical characteristics [1], [2]. Several factors can justify the pertinence of the present work. The most important ones are listed below:

1. Low power losses are desirable due to the increasing energy cost. Public awareness about environment makes energy conservation an actual and important issue that should be seriously considered.
2. Better EMI/EMC performance mainly due to the low conducted EMI.
3. Low electric stress across the components will reduce the risk of operation failure of the drive due to a broken component.
4. May decrease the unwanted effects of the coupling capacitances, decreasing the risk of motor failure.
5. Enhance of the overall performance of the motor drive system.

The efficiency problem is probably one of the most important issues on the design and development of frequency converters. The US Federal Energy Administration found out that in United States of America around 64% of the energy generation is only to be consumed by electrical motors [3]. The same document stated that approximately 28% of the total electrical consumption is due to commercial motor drives, utility power drives, municipal water pumps and residential motor drives. Quickly, we came to the conclusion that important amount of money and resources can be saved with small efficiency improvements on the motor drives. Thus, a slight improvement on the VSI efficiency can be significant in terms of energy saving during a long in-service life. Furthermore, the operation of the motor drive can be more efficient when the magnitudes of the low order voltage harmonics supplied to the motor are reduced and the energy savings will be even higher.

When we are referring to VSI, not only the high efficiency aspect should play an important role but also the quality of output line current should be taken in account. Low distorted current waveforms in the VSI output terminals are desirable in order to avoid as much as possible the de-rating of the motor and torque harmonics. A reduction of the harmonic content or THD (Total Harmonic Distortion) reduces losses in the induction motor and torque harmonics, especially at low speed region. The potentialities and advantages of a controllable DC-link voltage are evaluated in order to achieve all those previous aspects. A suitable combination of switching frequency and DC-link voltage magnitude is used to provide optimised pulse patterns, which should allow that the losses on the inverter part and the THD on the output line current can be kept within acceptable values for a determined steady state operating point. Off course all the good and bad results that can be retrieve by using this technique, must be carefully weighted, having in mind the overall efficiency off the AC drive system.

Nowadays, the simplest way to implement a variable DC bus voltage is by using an intermediate Buck-Boost converter stage between the rectifier stage and the inverter stage. This stage could not only control the DC-link voltage but also can work as a power factor corrector.

## Main circuit and simulator model

VSI's can be used in different kinds of applications where power conversion from DC (Direct Current) to AC (Alternate Current) is needed. AC motor drives commonly have two power conversion stages, the rectifier part and the inverter part. The rectification of the input AC voltage from the utility source by the rectifier will result in a DC voltage $V_{DC}$ (DC-link voltage). This voltage is composed by a constant component value and ripple due to the operation of the rectifier. This filtering stage is normally needed to reduce the ripple in the DC bus voltage. The most commonly used scheme for a three-phase inverter based on a two-level converter topology is the one shown in Fig. 1. FWD (Free Wheeling Diodes) also called anti-parallel diodes, are placed across the controllable switch in order to provide path for inductive currents. Until now the *pin* diode has been broadly used as a FWD in frequency converter applications. Nowadays a new kind of Schottky diode based on Silicon Carbide (SiC) has been developed [4]. This kind of Schottky diode, with high blocking voltage and with very small reverse recovery effect, can be a perfect choice to be used in the future with power converters operating at higher switching frequencies.

PWM mode of operation of the inverter switches is used to shape the fundamental output AC voltages to be as close as possible to a sine waveform with simultaneous amplitude control.

The implemented SIMPLORER® schematic diagram of the circuit in study is depicted in Fig. 1. The IGBT/FWD package was modelled using a commercially available IGBT component module (1MBI 600PX-120) from FUJI ELECTRIC. The package carries one IGBT and its FWD. A resume of the characteristic values used in the simulator model is shown in Table I.

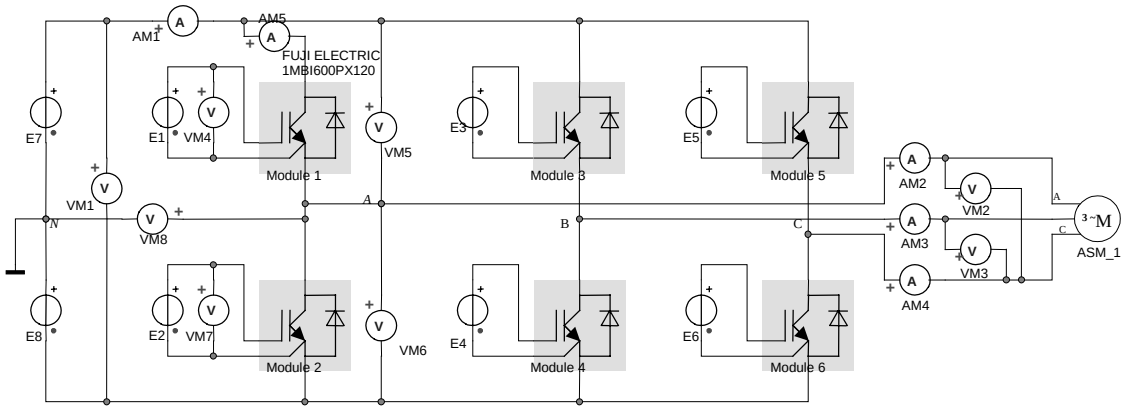



Figure 1. Implemented VSI schematic diagram in Simplorer®.

| Table I<br>**IGBT Module** (*Fuji Electric 1MBI 600PX-120*) | |
|---|---|
| Rated blocking voltage, $T_c = 25^oC$ | 1200 V |
| Rated current, $T_c = 25^oC$ | 600 A |
| Dynamic input ($dQ_G/dV_{GE}$), $T_j = 25^oC$ | 161,1 nC/V |
| Stray inductance ($L_\rho$) | 3 nH |
| Input stray capacitance ($C_{GE}$), $V_{CE} = 40V$ / $T_j = 25^oC$ | 60 nF |
| Output stray capacitance ($C_{CE}$), $V_{CE} = 0V$ / $T_j = 25^oC$ | 35 nF |
| Reverse transfer capacitance ($C_{CG}$), $V_{CE} = 40V$/ $T_j = 25^oC$ | 3 nF |
| Reverse recovering time ($t_{rr}$) | 0,325 μs |
| Duration of the tail current, $T_c = 125^oC$ | 0,45 μs |

Dynamic properties were achieved by adding to the static characteristics like internal resistances (forward resistances, $R_{on}$), stray capacitances ($C_{GE}$, $C_{CG}$ and $C_{CE}$). It is assumed that the temperature of operation remains constant, e.g., ambient ($T_c$) and junction temperature ($T_j$), 25°C and 125°C, respectively. This was done because the model does not support internal and external thermal temperature variations, e.g., self-heating. The transfer and the saturation curves of the FWD and IGBT were modelled by using the available catalogue data for the junction temperature of 125°C.

In SIMPLORER® the model of an induction (asynchronous) machine with squirrel-cage is available as lumped circuit component. The load torque can easily be controlled using arbitrary system variable, except quantities from the circuit module itself. So it is possible to simulate dynamic loads or to involve load conditions from the mechanical model part. The motor modelled in the schematic diagram is a three-phase squirrel cage induction motor with cast iron frame, manufactured by ABB Motors. A resume of the manufacture data and the data given by the simulator is listed in Table II. In the same table the list of parameters provided by SIMPLORER® using a supply voltage of 690 V is also given.

## VSI efficiency

Losses originating from the diodes and IGBT's of a VSI, can be explained by their internal conduction and switching mechanism. Thus, the efficiency of a switch-mode converter circuit is strongly dependent on the internal physical structure of the semiconductor switches. In fact, external factors like for instance the load power factor, stray inductances, gate-drive circuit and the modulation amplitude ratio $m_a$ play an important role. Conduction losses, also known as forward losses or even static losses, are depending on the forward resistance or on-state voltage drop of the component in use. Switching loss can be defined, as the energy spent by the controllable switch to change is conduction state from on to off or vice-versa. Those transitions cannot be done instantaneously but they take a certain time due to internal characteristics limitations of the switch. Those characteristics are called

dynamic characteristics. Besides the proportionality with the value of switching frequency $f_s$, internal stray capacitances play also an important role on the amount of energy lost on commutation process.

Table I
**Squirrel Cage Induction Motor** (*ABB motors M2BA 355 MLC 4)*

| | | |
|---|---|---|
| ABB data | Rated power | 500 kW |
| | Rated voltage | 400 V |
| | Rated current | 845 A |
| | Number of poles | 4 |
| | Rated speed | 1489 r.p.m. |
| | *Cos* $\varphi$ | 0,88 |
| | Synchronous speed | 1500 r.p.m. |
| | Rated torque | 3207 Nm |
| | Moment of inertia | 10,5 Kg.m$^2$ |
| | Efficiency with 100% of the load | 96,8 % |
| | Efficiency with 75% of the load | 96,8 % |
| SIMPLORER® data | Stator resistance | 4,8 mΩ |
| | Rotor resistance | 13,3 mΩ |
| | Stator leakage inductance | 172,6 μH |
| | Rotor leakage inductance | 202,22 μH |
| | Main inductance | 9,81 mH |
| | Rated power | 500 kW |
| | Rated voltage | 690 V |
| | Rated current | 460 A |
| | Number of poles | 4 |
| | Rated speed | 1477,6 r.p.m. |
| | *Cos* $\varphi$ | 0,92 |
| | Synchronous speed | 1500 r.p.m. |
| | Rated torque | 3207 Nm |
| | Moment of inertia | 10,5 Kg.m$^2$ |

## Analytical vs. simulation results

The analytical expressions (1), (2), (3), (4) and (5) derived in reference [5] are used in order to confirm the results obtained from computer simulations. Those expressions allow the calculation of losses in PWM inverter employing IGBT's. Several papers are dealing with the same subject [5]…[14]. However, reference [5] was found to be the most useful and straightforward in the analysis approach of IGBT losses. No additional practical measurements of the components are needed besides information from manufactures' catalogues. Conduction losses are derived separately for the IGBT and its FWD. The method presented in reference [5] is based on the calculation of energy loss in every pulse during a cycle. The derivation complexity of the expressions is reduced without greatly affecting accuracy by making the following assumptions:

1) Carrier frequency $f_s$ also known as switching frequency, is much higher than output frequency $f_1$ of the inverter. This means that high number of pulses per cycle is used. The carrier period $T_s$ is given by $1/f_s$ and the operating cycle period $T$ is given by $1/f_1$.
2) As a consequence of the first assumption, the phase current $i_A$ is considered to have a pure sinusoidal shape.
3) Steady-state operation.
4) Sinusoidal modulation with sine wave.
5) Operation at linear PWM region, $m_a \in [0,1]$.
6) Inductive load.

$$P_{IGBT1} = \left(\frac{1}{8} + \frac{m_a}{3\pi}\cos\varphi\right) R_{on} I_{C(M)}{}^2 + \left(\frac{1}{2\pi} + \frac{m_a}{8}\cos\varphi\right) V_{CE(0)} I_{C(M)} \quad (1)$$

$$P_{FWD1} = \left(\frac{1}{8} - \frac{m_a}{3\pi}\cos\varphi\right) R_{on} I_{C(M)}{}^2 + \left(\frac{1}{2\pi} - \frac{m_a}{8}\cos\varphi\right) V_{F(0)} I_{C(M)} \quad (2)$$

$$P_{on} = \frac{1}{8} V_{DC} t_{r(N)} \frac{I^2{}_{C(M)}}{I_{C(N)}} f_s \quad (3)$$

$$P_{off} = V_{DC} I_{C(M)} t_{f(N)} \left(\frac{1}{3\pi} + \frac{1}{24}\frac{I_{C(M)}}{I_{C(N)}}\right) f_s \quad (4)$$

$$P_{rr} = f_s V_{DC} \left\{ \left[ 0,28 + \frac{0,38}{\pi}\frac{I_{C(M)}}{I_{C(N)}} + 0,015\left(\frac{I_{C(M)}}{I_{C(N)}}\right)^2 \right] Q_{rr(N)} + \left(\frac{0,8}{\pi} + 0,05\frac{I_{C(M)}}{I_{C(N)}}\right) I_{C(M)} t_{rr(N)} \right\} \quad (5)$$

Where:

| | | | |
|---|---|---|---|
| $f_s$ | Switching frequency | $I_{C(M)}$ | Peak value of the load current |
| $I_{C(N)}$ | Nominal current of the IGBT | $m_a$ | Amplitude modulation ratio |
| $P_{FWD}$ | Conduction loss of the FWD | $P_{IGBT}$ | Conduction loss of the IGBT |
| $P_{off}$ | Turn-off loss | $P_{on}$ | Turn-on loss |
| $P_{rr}$ | Reverse recovery loss | $Q_{rr(N)}$ | Nominal reverse recovery charge |
| $t_{f(N)}$ | Nominal fall time of the current | $t_{r(N)}$ | Nominal rise time of the current |
| $t_{rr(N)}$ | Nominal reverse recovery time | $V_{DC}$ | DC-link voltage |
| $\cos\varphi$ | Load power factor | | |

The results of the above analytical expressions are compared with the results of simulations. The comparison was done using the same operating points, where the fundamental value of the output voltage and the operating frequency are constant. In most cases operation at 5 Hz output frequency only has been studied. One study includes six operating points. Relation of output frequency and output voltage is seen from Fig. 2., i.e. it is constant.

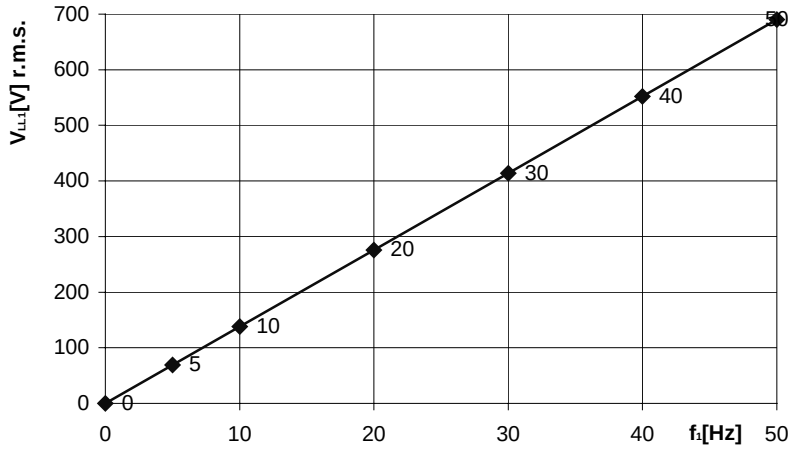



Figure 2. Operating points used (Scalar control).

The simulation results presented in this work are performed with constant gate circuit conditions. This option is essential in order to have a systematic basis of comparison and evaluation on the effects of changes of the DC-link voltage magnitude in the VSI performance. A normal gate-drive circuit with a

DC voltage source and a gate resistance is used in the VSI circuit implementation. The variation of $v_{GE}$ signal is between +15V(on-state) and –5V (off-state). The value of gate resistor, which will influence the commutation speed of the IGBT, i.e., the turn on and turn off time ($t_{on}$, $t_{off}$), was chosen to be 15Ω. This high value of $R_G$ allows longer switching transitions. That fact is beneficial because it will permit a better representation of those periods due to the high number of points calculated within that period. No more additional considerations were taken to choose the value of $R_G$, besides that the operation of the IGBT should remain within its SOA.

## Operation at 5 Hz output frequency

For each operation point, several simulations were carried out for different combinations of switching frequencies and DC-link voltage values. Finally, the same operation conditions were applied to the analytical expressions and the inverter total losses were compared. Fig. 3 shows a comparison between analytical and simulation results for the operating frequency of 5 Hz. The values of the DC-link used were 931,5V (maximum value) and 200V (value which still allow the operation inside the linear PWM region, were the analytical expressions are valid). The switching frequency was 75Hz and 9kHz.

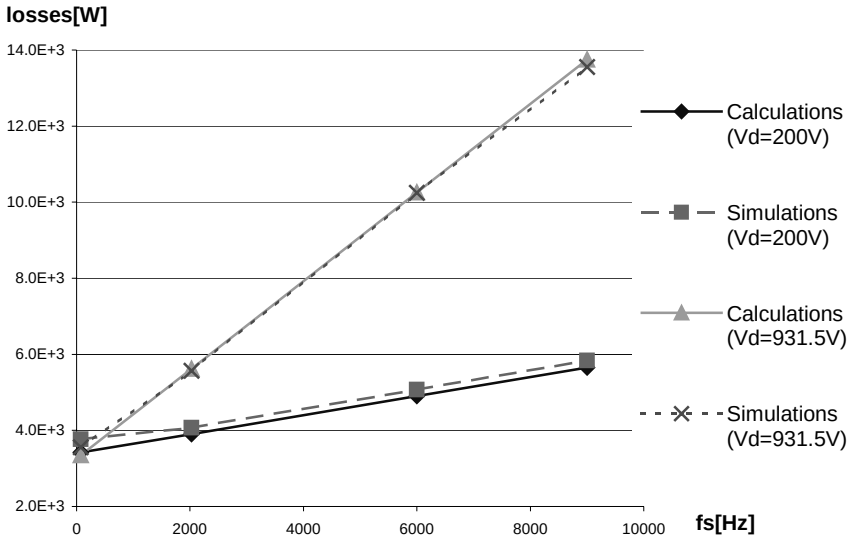
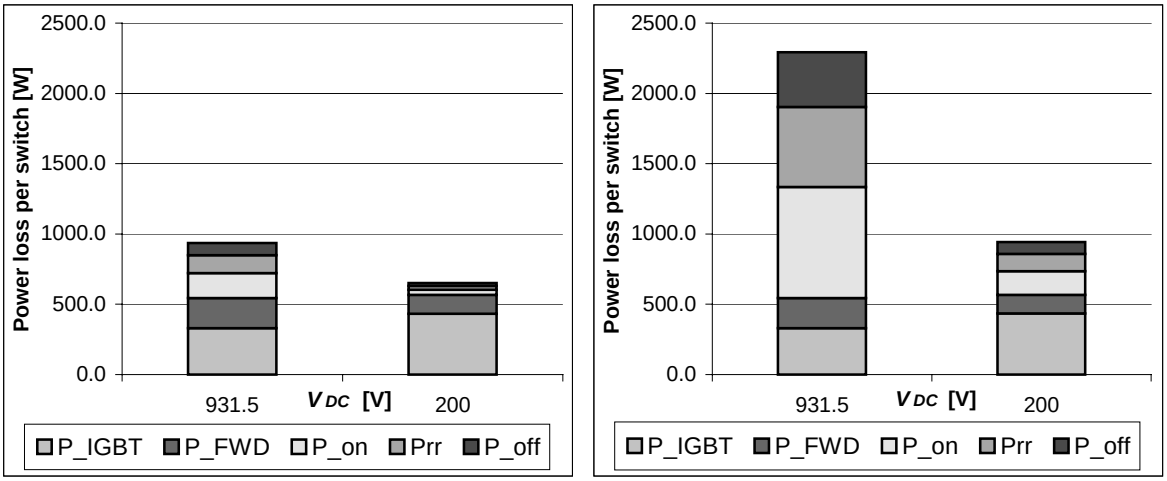



Figure 3. Analytical losses vs. simulation losses; $f_1$ = 5 Hz, full load.

To know the influence of the relative error on the efficiency results, the maximum relative error (≅10%) obtained, is used. That error was obtained at $f_s$ = 75 Hz, $f_1$ = 5 Hz, full load and $V_{DC}$ = 200 V with a constant inverter output power of 54 kW. It turns out that the efficiency difference due to the error is around 0,65%. Assuming that no higher relative value is possible that means that all values of efficiency will have an error margin equal or smaller than ±0,65%.

Assuming the truthfulness and accuracy of the derived analytical expressions, they are used to determine the distribution of the different type of losses inside the IGBT module. It is clear that those losses are representing as well the total loss distribution of the VSI, considering the respective proportionality (6 IGBT modules). Fig. 4 shows the evolution and the distribution of different losses inside the switch module.

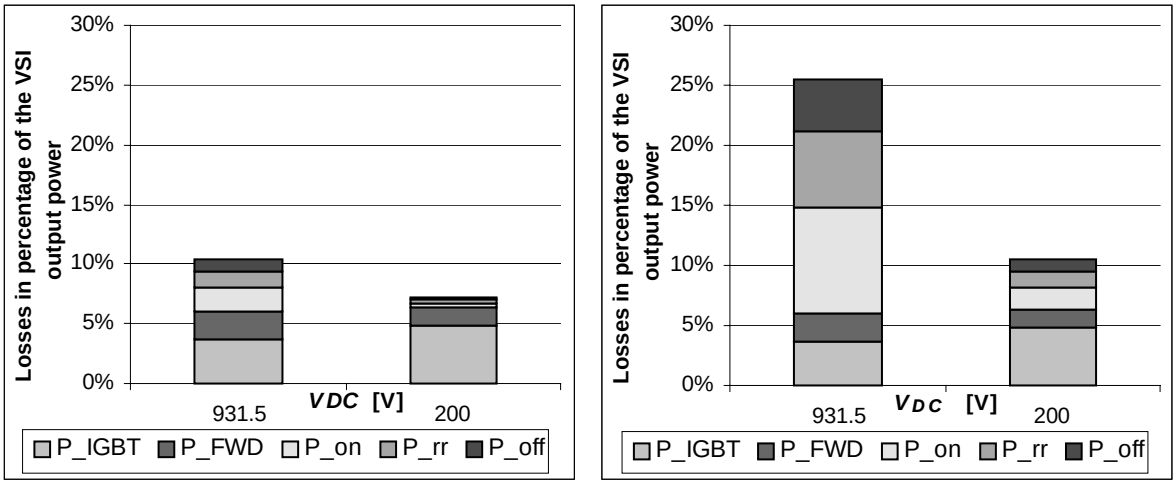



a) b)

Figure 4. Influence of the DC-link voltage on the distribution of different types of losses in the VSI switches at $f_1$ = 5 Hz and with full load: a) $f_s$ = 2 kHz; b) $f_s$ = 9 kHz.

Again the comparison is done for the same operating point and two different magnitudes of the DC-link voltages $V_{DC}$ (931,5 V, 200 V). For those conditions, two switching frequencies were used (2 kHz, 9 kHz). The results are depicted in Figs. 4a and b. The distribution of losses shows that for lower switching frequencies, e.g. 2 kHz, the conduction losses are slightly increasing when $V_{DC}$ is lowered. Also is confirmed that the IGBT is contributing with the major part of the conduction losses at low $V_{DC}$. This is because of its higher on-state voltage drop in comparison with the FWD. Lowering the DC-link voltage has a strong impact on the switching losses ($P_{on}$ + $P_{rr}$ + $P_{off}$), which are clearly reduced.

Another way to compare the distribution is to refer them to the same constant output power of the VSI. Fig. 5 represents the different types of losses in percentage of the constant output power of the VSI. In that way the total amount of losses between the different DC-link voltages can be easily compared. Again the comparison is done for the same operating point at different $V_{DC}$ and $f_s$. Also here the increase of conduction losses due to the increase of modulation amplitude $m_a$ is not decisive. This is so because the reduction on the switching losses is significant and can easily compensate for the small increase of conduction losses as shown in Fig. 5a,b.




a) b)

Figure 5. Influence of the DC-link voltage on the distribution of the different type of losses referred to the output power of the VSI at $f_1$ = 5 Hz and with full load: a) $f_s$ = 2 kHz; b) $f_s$ = 9 kHz.

Operating the VSI with a switching frequency of 9 kHz and full DC-link voltage (931,5 V) at $f_1$ = 5 Hz, will originate losses, which are 25 % of output power, as shown in Fig. 5b. Decreasing the DC-link voltage to 200 V, using the same switching frequency, losses are reduced to 10 %. It means that 15% of the power loss can be saved, yielding a reduction of more than 50% of the initial losses (c.f. Fig. 5b). The main aspect retrieved from Fig. 5 is the reduction of the total amount of losses at high switching frequencies. It is interesting to realize that operating at $f_s$ = 2 kHz, $V_{DC}$ = 931,5 V generates almost the same losses than operating at higher switching frequency $f_s$ = 9 kHz with lower DC-link voltage $V_{DC}$ = 200 V. This last observation makes clear that lowering the DC-link voltage especially at low speeds can be very useful also in terms of efficiency.

High voltage derivatives across the IGBT's due to high magnitude of the DC-link voltage will decrease the parasitic transfer capacitance $C_{CG}$ owing to its voltage dependence. Thus, a low gradient of $v_{CE}$ at turn-on or turn-off ($dv_{CE}/dt$), is mainly dependent on the time constant define by the $C_{CG}$ and the gate resistor $R_G$ values. Considering a constant value of the gate resistor, which implies a constant gate current to discharge $C_{CG}$, it is easy to realize that for higher values of $V_{CE}$, the discharging time of $C_{CG}$ will be fast because of its smaller capacitance that implies a lower time constant ($R_G \times C_{CG}$). Using as an example case the turn-on transient, the derivative ($dv_{CE}/dt$) will be high mainly because $V_{CE}$ is high and the fall time $t_f(v_{CE})$ is short due to the low time constant. This situation is depicted in Fig. 6a.

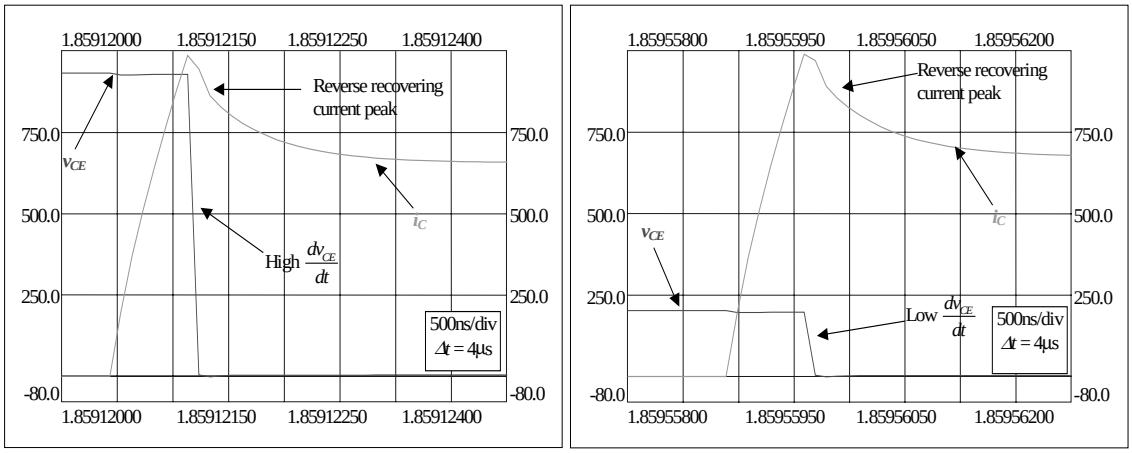



Figure 6. Turn-on waveforms, $f_s$ = 2 kHz, $f_1$ = 5 Hz (127 r.p.m.), full load: a) $V_{DC}$ = 931,5 V; b) $V_{DC}$ = 200V.

If a decreased value of the DC-link is used, meaning low $v_{CE}$, $C_{CG}$ value increases proportionally. Due to the increased value of $C_{CG}$ the time constant ($R_G \times C_{CG}$) will also increase making the $t_f(v_{CE})$ longer. Therefore, the derivative will be low when compared with the previous situation. The lower voltage switching is represented in Fig. 6b. When both above referred figures are compared one can note that the interception area between $i_C$ and $v_{CE}$ waveforms is much larger for high DC-link voltage than for the lower value. This represents approximately the value of the power lost at turn-on. To be more accurate the interception area comprises a part due to recovery losses of the FWD.

The 3D plan in Fig. 7 is based on the simulation results and it shows the evolution of the VSI efficiency with the switching frequency $f_s$ and DC-link voltage $V_{DC}$. It can be easily noted that if high switching frequencies need to be used, it is convenient to decrease the value of the DC-link voltage in order to improve the VSI efficiency.

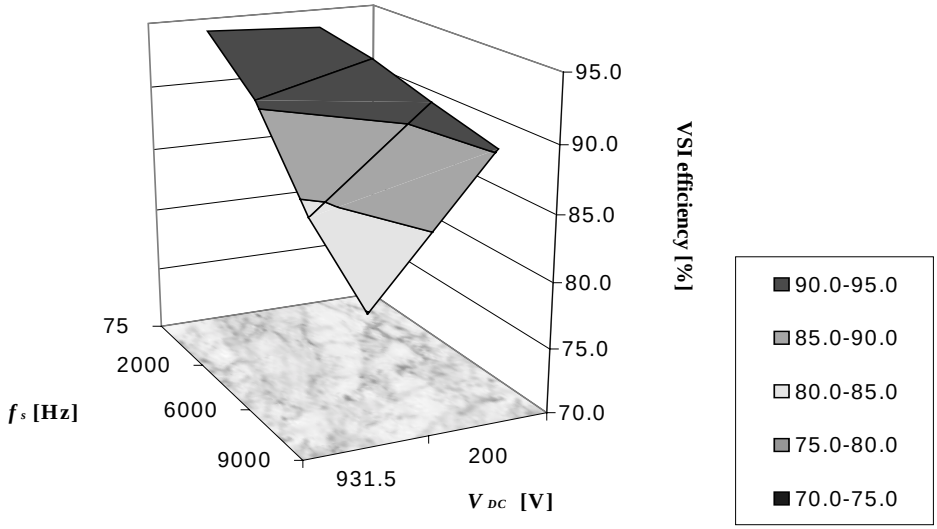



Figure 7. Efficiency vs. DC-link voltage and switching frequency ($f_1$ = 5Hz, full load).

## Operation with variable output frequency

The results presented until known were for an operating frequency of 5 Hz. Fig. 8 shows the VSI efficiency evolution throughout the speed range. Frequency and voltage values are those presented in Fig. 2. It can be noted that if the lowest possible DC-link voltage is used the efficiency value increases. That fact is more obvious at low speed region as was expected and discussed before. It should be noted that for higher switching frequencies the efficiency gap at low speed is expected to be wider.

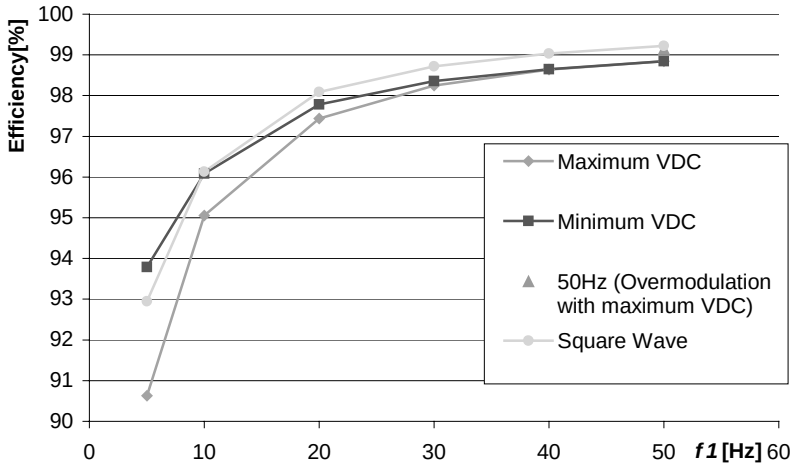



Figure 8. PWM ($f_s$ = 2 kHz) and SW VSI efficiency vs. inverter output frequency at maximum and minimum DC-link voltage and full load (constant).

The SW (Square Wave) operation has during the major part of the speed range better efficiency than the PWM. At low speeds the efficiency decreases, due to the fact that losses are maintaining almost the same value whilst the output power is decreasing considerably. This can be better verified in the Fig. 9, which shows the total amount of losses at different speeds and $V_{DC}$ for the PWM and SW inverter. In this figure the operation is at $f_1$ = 50 Hz and the linear region is used.

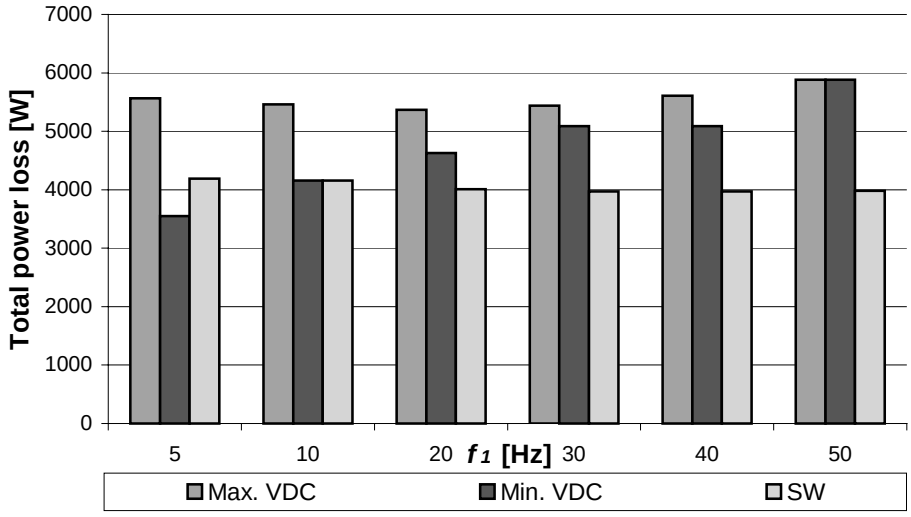



Figure 9. Total losses for the PWM ($f_s$ = 2kHz) and SW inverter operating at constant full load vs. the VSI output frequency and DC-link voltage variation.

## Conclusions

From the overall analysis of the entire work, it can be concluded that an intermediate controllable DC-link voltage stage can be very useful in improving the efficiency of a PWM VSI, especially at higher values of switching frequency. It is clearly noted from the analytical and simulation results that the switching losses could be significantly reduced if a low DC-link voltage is used. If higher switching frequencies can be used the physical dimension of filters can be reduced and the efficiency of the driven motor will be slightly increased. Also, improvement on the motor efficiency due to the lower contents of harmonics currents in the output current fed to motor can also be achieved. This will reduce the heat in the windings. Moreover, by using low value of DC-link voltage, the motor over voltage effect caused by the output voltage pulses transmitted along the cable connecting the VSI to the motor, can also be reduced. This will reduce the aging effect of the motor stator insulation, which is one of the causes for motor failing.

The THD of the output current fed to the motor did not show great additional benefits by decreasing the DC-link voltage, except for low switching frequencies. THD was one of the aspects under investigation during this work because induction motors are normally over-rated (more costly) in order to cope with the harmonics fed by the inverter due to switch-mode of operation. Moreover, temperature can be related with the expected lifetime of the motor. Therefore, a minimum value of $THD_i$ is wanted. Operating the VSI with square (SW) modulation reveals higher $THD_i$ value and torque ripple. The efficiency was approximately the same as in the linear PWM operation with the lowest DC-link voltage.

Square-wave inverters are good choices in applications were low dynamic performance is enough. In that case a buck-boost PWM rectifier with power factor capabilities can be an interesting option to supply the required variable DC-link voltage. In applications of hundreds of kilowatts, the main difficulty can be the high DC-link current required from the buck-boost PWM rectifier that will create high conduction losses and decrease efficiency. The implementation of a controllable DC-link circuit along with PFC (Power Factor Correction), which is beyond the scope of this work, is an interesting topic for future studies.

Electromagnetic Compatibility (EMC) should be considered before and during the designing stage of a frequency converter. Electromagnetic Interference (EMI) can be reduced if low DC-link voltages are used due to the *dv/dt* gradient in the output voltage. In the VSI the EMI comes also partially from the reverse recovery current of the FWD. Unfortunately, the change of the DC-link voltage to low values

hasn't revealed any decrease on the reverse recovery peak current of the FWD in spite of the reduction of the reverse recovery power losses. In the future, this problem can be very much attenuated if IGBT package for high power applications were made replacing the commonly used *pin* FWD by the new Silicon Carbide (SiC) diodes. SiC diodes don't have reverse recovery current and they have low reverse recovery charge $Q_{rr}$. Hopefully, the operation of this kind of switch combined with a controlled DC-link voltage could allow substantial reductions on switching losses, which can be very useful at high switching frequency operation, yielding high efficiency of the VSI with improved EMI characteristics.

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