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# Weak-Grid Tolerant Positive- and Negative-Sequence Current Control of Voltage-Source Converters

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Abstract—This paper deals with positive- and negativesequence current control of voltage-source converters. An enhanced weak-grid tolerant state-feedback controller design based on direct pole placement approach is proposed. The controller is synthesized from a body of literature on multi-frequency current control of grid converters. The resulting design yields consistent dynamic performance for varying grid strengths, and remains stable even under very weak grids. Due to the explicit parameterization of the pole locations, complex optimization methods often associated with robust control designs are avoided, which simplifies the controller design process.

Index Terms—Current control, grid converter, negative sequence, state-feedback control, weak grid

### I. INTRODUCTION

The ongoing clean energy revolution drives the proliferation of renewable energy sources in the electric grid. Consequently, an increasing share of generated power is processed through power-electronic converters that act as an interface between the renewable energy sources and the grid. Due to the uncertain and time-varying nature of the grid impedance, the interfacing converters should be designed robust to variations in the grid impedance. Furthermore, as the share of power production through grid converters increases, demand for additional ancillary services provided by them, e.g., grid fault support, grows. In recent standards, e.g., [1], features such as positive- and negative-sequence reactive current support is required from grid converters under fault conditions.

Several different control strategies for multi-frequency current control, which the positive- and negative-sequence current control is a special case of, have been proposed recently [2]– [18]. An interesting subset of these controllers are those based on the state-feedback design, which has been proven effective and flexible for control of grid converters [4]–[18]. The designs of such controllers can be roughly divided into direct [4]–[6] and indirect [7]–[18] pole placement approaches.

In the direct pole placement approaches [4]–[6], the closedloop poles are explicitly parameterized, and the state-feedback gains are computed based on the desired locations. In [4], the design is based on setting the real parts of the poles equal while leaving the imaginary parts unmodified. The value of the real part is determined so as to retain stability under predefined parameter variations in the filter and grid inductances. While this approach is simple as the pole placement is determined by a single parameter, the design is based on relatively mild variations in the inductance value, and the performance of the system is not comprehensively analyzed. In [5], a positiveand negative-sequence current control design is presented based on a disturbance observer, and an equivalent integratorbased approach is shown in [6]. These designs focus on the aspect of dynamic performance under nominal conditions, with emphasis on the reference tracking. The resulting designs are shown to tolerate only moderate variations in the grid inductance [5].

In the indirect pole placement approaches [7]–[18], the closed-loop poles are placed indirectly by choosing the state-feedback gains through optimization. Various optimization methods for computing the state-feedback gains have been proposed, e.g., linear quadratic regulator (LQR) design [7]–[11], linear matrix inequality (LMI) optimization [12], [13], combination of LQR and LMI [14], combination of a genetic algorithm (GA) and LMI [15], particle swarm optimization [16],  $\mathcal{H}_{\infty}$  design [17], and steady-state Kalman filter design [18]. By examining the collection of pole maps produced by these methods, a clear trend can be observed. The closed-loop poles, excluding any resonant poles in the controlled system and the computational delay pole, tend to be located near their open-loop locations in the majority of the designs.

Conventionally, maintaining the closed-loop poles adjacent to their open-loop locations has been considered as a good design approach, since this maintains the state-feedback gains and, consequently, the control effort low [19]. Furthermore, low values of control gains are tied to enhanced system robustness to parameter variations [20]. On the flipside, when majority of the poles are near the unit circle, the dynamic performance tends to be severely hindered as compared to, e.g., the designs based on direct pole placement approach [4]– [6]. Consequently, there is a trade-off between robustness to parameter variations and dynamic performance [19], [20].

Motivated by the glaring similarities between the different indirect pole placement approaches for multi-frequency current controllers, this paper proposes an enhanced direct pole placement design for positive- and negative-sequence current control of grid converters. The design is synthesized from the existing body of literature on multi-frequency current control. Assuming a dominantly inductive grid impedance, the goal



Fig. 1. (a) Block diagram of a grid converter equipped with an L filter. CC and PLL are abbreviations of current controller and phase-locked loop, respectively. Superscript s indicates signals in stationary coordinates. (b) Block diagram of the positive- and negative-sequence state-feedback current controller.

of the design is to achieve high tolerance to grid inductance variations, resulting in stable operation even under short-circuit ratio (SCR) of unity, while avoiding the complex optimization routines typically associated with robust control designs. The results are validated experimentally with a 12.5-kVA grid converter.

## **II. PRELIMINARIES**

Fig. 1(a) shows a three-phase grid converter system connected through an L filter to an electric grid modeled as a dominantly inductive impedance  $Z_{g}^{s}(s)$  and an ideal voltage source  $e_{g}^{s}$ . The system is analyzed using space vectors in synchronous coordinates, e.g., the current is  $i_{c} = i_{cd} + ji_{cq}$ . Signals in stationary coordinates are denoted with superscript s, e.g., the converter voltage is  $u_{c}^{s} = u_{c\alpha} + ju_{c\beta}$ .

## A. System Model

In the control design stage, the resistive losses are omitted, i.e., the filter resistance is considered to be zero. Consequently, the continuous-time model of the L filter in synchronous coordinates rotating at the angular frequency  $\omega_{\rm g}$  is given by

$$\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{\mathrm{c}} = -\mathrm{j}\omega_{\mathrm{g}}\boldsymbol{i}_{\mathrm{c}} + \frac{1}{L_{\mathrm{f}}}\boldsymbol{u}_{\mathrm{c}} - \frac{1}{L_{\mathrm{f}}}\boldsymbol{u}_{\mathrm{g}}$$
(1)

where  $u_{\rm g}$  is the voltage at the point of common coupling (PCC) and  $L_{\rm f}$  is the filter inductance. Assuming that the pulse-width modulator (PWM) is modeled as a zero-order hold (ZOH) in stationary coordinates and that the currents are sampled in synchronism with the PWM, the hold-equivalent model of the system (1) can be written as

$$i_{\rm c}(k+1) = \phi i_{\rm c}(k) + \gamma u_{\rm c}(k) - \gamma u_{\rm g}(k)$$
 (2)

where  $\phi = \exp(-j\omega_{\rm g}T_{\rm s})$ ,  $\gamma = \phi T_{\rm s}/L_{\rm f}$ , and  $T_{\rm s}$  is the sampling period. Due to the finiteness of computational resources available in practical control hardware, a computational delay of one sample is incurred in the control system, i.e.,

$$\boldsymbol{u}_{\rm c}(k+1) = \boldsymbol{\phi} \boldsymbol{u}_{\rm c,ref}(k) \tag{3}$$

where  $\phi$  is a phase angle shift due to the delay. The SCR of the system is defined as

$$SCR = \frac{L_{b}}{L_{f} + L_{g}}$$
(4)

where  $L_{\rm b}$  is the base value of the inductance and  $L_{\rm g}$  is the grid inductance.  $L_{\rm b}$  is obtained from the base impedance  $Z_{\rm b}$  and the nominal angular frequency  $\omega_{\rm g}$  as  $L_{\rm b} = Z_{\rm b}/\omega_{\rm g}$ .

# B. Positive- and Negative-Sequence Current Control

A block diagram of the positive- and negative-sequence state-feedback current controller presented in [6] is shown in Fig. 1(b). In the figure,  $i_{c,ref}^+$  and  $i_{c,ref}^-$  are the positive- and negative-sequence current references, respectively. In accordance with the figure, the control law can be written as

$$\boldsymbol{u}_{\rm c,ref}(k) = \boldsymbol{k}_{\rm t}^{+} \boldsymbol{i}_{\rm c,ref}^{+}(k) + \boldsymbol{k}_{\rm t}^{-} \boldsymbol{i}_{\rm c,ref}^{-}(k) + \boldsymbol{k}_{\rm i}^{+} \boldsymbol{x}_{\rm i}^{+}(k) + \boldsymbol{k}_{\rm i}^{-} \boldsymbol{x}_{\rm i}^{-}(k) - \boldsymbol{k}_{1} \boldsymbol{i}_{\rm c}(k) - \boldsymbol{k}_{2} \boldsymbol{u}_{\rm c}(k)$$
(5)

where  $k_t^+$  and  $k_t^-$  are the reference feedforward gains,  $k_i^+$ and  $k_i^-$  are the integral gains, and  $k_1$  and  $k_2$  are the statefeedback gains. The integral states  $x_i^+$  and  $x_i^-$  for positiveand negative sequences, respectively, are defined as [6]

$$\begin{aligned} \boldsymbol{x}_{i}^{+}(k+1) &= \boldsymbol{x}_{i}^{+}(k) + \boldsymbol{i}_{c,ref}^{+}(k) + \boldsymbol{k}_{c}^{-}\boldsymbol{i}_{c,ref}^{-}(k) - \boldsymbol{i}_{c}(k) & (6) \\ \boldsymbol{x}_{i}^{-}(k+1) &= \boldsymbol{\varphi}\boldsymbol{x}_{i}^{-}(k) + \boldsymbol{i}_{c,ref}^{-}(k) + \boldsymbol{k}_{c}^{+}\boldsymbol{i}_{c,ref}^{+}(k) - \boldsymbol{i}_{c}(k) & (7) \end{aligned}$$

where  $\varphi = \exp(-j2\omega_g T_s)$  and  $k_c^+$  and  $k_c^-$  are the reference decoupling gains. While these decoupling gains are atypical, their inclusion is justified, since they can be used to decouple the positive- and negative-sequence referencetracking dynamics, resulting in performance equivalent to a disturbance-observer-based implementation [6]. In general, the integral states are used to eliminate the steady-state referencetracking error of the positive- and negative-sequence currents that correspond to the dc and  $-2\omega_g$  frequency components in synchronous coordinates, respectively [21]. In the analysis, the possibility of actuator saturation, which tends to result in integral wind-up, is omitted. However, a realizable-reference anti-windup is implemented for both integrators in the experiments [22]. *Remark 1:* Several of the well-established harmonic compensators can be obtained as special cases of (6) and (7). For example, the reduced-order generalized integrators (ROGIs) [23] can be realized by selecting  $\mathbf{k}_c^+ = \mathbf{k}_c^- = 0$ . In addition, the classical resonator [4] can be realized by selecting  $\mathbf{k}_i^+ = \mathbf{k}_i^-$  and  $\mathbf{k}_c^+ = \mathbf{k}_c^- = 0$ .

# III. SYNTHESIZED DIRECT POLE PLACEMENT

The system presented in the previous section is of fourth order, i.e., there are four poles. These poles can be extracted, e.g., by formulating a state-space model of (2), (3), (6), and (7), and computing the eigenvalues of the resulting system matrix. The open-loop poles are obtained as

The pole  $p_{10}$  originates from the computational delay (3), the pole  $p_{20}$  from the *L* filter (2), and the poles  $p_{30}$  and  $p_{40}$  from the integrators (6) and (7), respectively. The closed-loop system, which is obtained by applying the control law (5) on the open-loop system, can be written as

$$i_{\rm c}(z) = G_{\rm cl}^+(z)i_{\rm c,ref}^+(z) + G_{\rm cl}^-(z)i_{\rm c,ref}^-(z) - Y_{\rm cl}(z)u_{\rm g}(z)$$
 (9)

where  $G_{\rm cl}^+(z)$  and  $G_{\rm cl}^-(z)$  are the reference-tracking transfer functions and  $Y_{\rm cl}(z)$  is the output admittance from the PCC voltage  $u_{\rm g}$ , which considered as a disturbance. The application of the control law alters the locations of open-loop poles (8) based on the choice of the gains  $k_i^+, k_i^-, k_1$ , and  $k_2$ . Consequently, the characteristic polynomial of the closed-loop system can be written as

$$D(z) = (z - p_{1c})(z - p_{2c})(z - p_{3c})(z - p_{4c})$$
(10)

where  $p_{1c,2c,3c,4c}$  are the closed-loop pole locations. The reference-tracking transfer functions  $G_{cl}^+(z)$  and  $G_{cl}^-(z)$  can be written as

$$G_{\rm cl}^{+}(z) = \frac{i_{\rm c}(z)}{i_{\rm c,ref}^{+}(z)} = \frac{\phi \gamma k_{\rm t}^{+}(z - z_{1}^{+})(z - z_{2}^{+})}{D(z)}$$
(11)

$$G_{\rm cl}^{-}(z) = \frac{i_{\rm c}(z)}{i_{\rm c,ref}^{-}(z)} = \frac{\phi \gamma k_{\rm t}^{-}(z - z_{1}^{-})(z - z_{2}^{-})}{D(z)}$$
(12)

respectively, where  $z_{1,2}^{+/-}$  are the reference-tracking zeros. The locations of the zeros in (11) depend on the gains  $k_t^+$  and  $k_c^+$ . Analogously, the locations of the zeros in (12) depend on the gains  $k_t^-$  and  $k_c^-$ . Closed-form equations for these gains as functions of the desired zero locations are given in [6]. The output admittance of the system can be written as

$$Y_{\rm cl}(z) = \frac{\boldsymbol{i}_{\rm c}(z)}{\boldsymbol{u}_{\rm g}(z)} = \frac{\phi \gamma(z - \boldsymbol{z}_{\rm s})(z - 1)(z - \boldsymbol{\varphi})}{\boldsymbol{D}(z)}$$
(13)

where  $z_s$  is a sampling zero originating from the discretization of the *L* filter [20]. The two other static zeros originate from the integrators, and they locate identically to the open-loop integrator poles  $p_{3o}$  and  $p_{4o}$ .

In the following, the proposed direct pole placement design is presented, starting with the design of reference tracking, followed by the design of disturbance rejection. Since the evaluation of system robustness to grid inductance variations is not possible until all the poles have been selected, an initial pole parameterization is formulated first. Subsequently, it is shown that a large set of parameter values for the pole parameterization results in a robust design.

### A. Reference Tracking

Since the two zeros in the reference-tracking transfer functions (11) and (12) can be placed freely, two pole-zero cancellations can be achieved. Consequently, the reference-tracking dynamics under nominal conditions depend only on the two remaining poles. In the following, the reference-tracking zeros  $z_1^{+/-}$  and  $z_2^{+/-}$  are assumed to be placed on the poles  $p_{3c}$  and  $p_{4c}$ . This results in reference-tracking transfer functions

$$G_{\rm cl}^{+/-}(z) = \frac{\phi \gamma k_{\rm t}^{+/-}}{(z - p_{\rm 1c})(z - p_{\rm 2c})}.$$
 (14)

The task is then to define the remaining closed-loop poles  $p_{1c}$  and  $p_{2c}$  to completely determine the reference-tracking dynamics. The approach taken below is based on [5], [6]. However, similar results can also be found in the indirect designs [13], [15], [17].

Contrary to the other open-loop poles that locate on the unit circle, the pole  $p_{1o}$  is located in the origin of the complex z-plane. The origin is a special point, since no point from the complex s-plane maps to it through the mapping  $z = \exp(-sT_s)$  that links the continuous- and discrete-time complex planes [21]. In fact, the dynamic mode corresponding to the pole in the origin has the minimum settling time in the discrete-time domain [20]. Since this pole does not impose limitations on the bandwidth of the closed-loop system, it is initially left in its open-loop location, i.e,

$$\boldsymbol{p}_{1\mathrm{c}} = \boldsymbol{p}_{1\mathrm{o}}.\tag{15}$$

As a consequence of this choice, the pole  $p_{2c}$  then sets the bandwidth of reference tracking. Unless the pole is placed on the real axis, the reference-tracking dynamics will be oscillatory in nature [21], as non-zero imaginary parts in poles translate into oscillatory transients. As such transients are not desirable due to overshoots, the location of  $p_{2c}$  is constrained to the real axis, i.e.,

$$\boldsymbol{p}_{2c} = \exp(-\alpha_c T_s) \tag{16}$$

where  $\alpha_c$  defines the reference-tracking bandwidth.

The resulting reference-tracking dynamics are approximately of first-order under nominal conditions, and the rise time of the system with bandwidth  $\alpha_c$  is defined as  $t_r = 2.2/\alpha_c$ . The two other poles that largely determine the robustness of the system to grid inductance variations, are determined in the next section.

# B. Disturbance Rejection

Under nominal conditions, the poles  $p_{3c}$  and  $p_{4c}$  do not affect the reference-tracking dynamics. Therefore, they can be used to shape the output admittance (13) of the system, which



Fig. 2. Contour map of grid inductance values  $L_{\rm g}$  for which the system turns unstable, shown as a function of the design parameters  $\zeta$  and  $\beta_{\rm c}$ . In the figure,  $\alpha_{\rm c} = 8$  p.u. The blue cross depicts the example tuning with  $\beta_{\rm c} = 4\alpha_{\rm c}$  and  $\zeta = 0.15$  used in the results section.

determines the system response to grid-voltage disturbances. In the indirect pole placement approaches [7]–[18], the corresponding poles tend to be located near the unit circle, close to the open-loop locations of the integrator poles.

By examining the loop gain of the system, it can be shown that as the grid inductance increases, the closed-loop poles traverse towards their open-loop locations. This happens because as the grid inductance increases, the gain of the system decreases. Consequently, the effectiveness of the constant-gain feedback decreases. Since the locus of a pole adjacent to its open-loop location behaves analogously to the electric field of a dipole [24], the length of the locus is typically in proportion to the distance between the pole and its open-loop location, i.e., short. Consequently, the movements of the pole tend to be minor for variations in the grid inductance. Placing a pole near one of the open-loop poles at the unit circle causes a partial pole-zero cancellation in the output admittance (13), which effectively reduces the disturbance rejection capability around the frequencies of the partially canceled zero. In the interest of maintaining good disturbance rejection for frequencies around the fundamental frequency, pole placement near the open-loop negative-sequence integrator pole is considered. To provide additional flexibility, a radial projection approach is adopted [21]. The pole  $p_{3c}$  is given by

$$\boldsymbol{p}_{\rm 3c} = \exp[-(\zeta + j\sqrt{1-\zeta^2})2\omega_{\rm g}T_{\rm s}] \tag{17}$$

where  $\zeta$  is the damping ratio of the pole. Radial projection allows for adjusting the real part of the pole while maintaining a constant natural frequency of  $-2\omega_{\rm g}$ . The pole  $p_{\rm 4c}$ , on the other hand, is given by

$$\boldsymbol{p}_{\rm 4c} = \exp(-\beta_{\rm c} T_{\rm s}) \tag{18}$$

where  $\beta_c$  is a tuning parameter. This choice is based on preserving the dynamic performance of the system, e.g., in recovering from grid-voltage disturbaces, while still meeting the requirement of stability for grid inductance values corresponding to the SCR of unity.

*Remark 2*: as shown in [25], the introduction of additional outer loop controllers can have an adverse effect on the stability of the system. These issues can potentially be alleviated



Fig. 3. Pole map of the two reference designs based on the indirect approach in [8] (top) and the direct approach in [5] (middle), respectively, and of the proposed design (bottom). In the proposed pole placement, the parameter values are selected as  $\zeta = 0.15$  and  $\beta_c = 4\alpha_c$ . Nominal pole locations are marked in black, with star symbol referring to a double pole.

through reduction of  $\beta_c$ , but this analysis is a topic for future research.

*Remark 3:* While the filter is assumed purely inductive above, the findings are equally applicable to systems equipped with LCL filters instead of an L filter. The additional resonant poles of the LCL filter could be placed, e.g., by using the radial projection technique [cf. (17)].

### **IV. RESULTS**

In the following section, the base values are selected as the nominal values of a 12.5-kVA 50-Hz grid converter system with  $i_{\rm n} = \sqrt{2} \cdot 18$  A and  $u_{\rm b} = \sqrt{2/3} \cdot 400$  V. Consequently, the base impedance becomes  $Z_{\rm b} = 12.6 \Omega$ . The filter inductance is  $L_{\rm f} = 5$  mH (0.12 p.u.) and a switching frequency of  $f_{\rm sw} = 4$  kHz is used. The sampling frequency is  $f_{\rm s} = 2f_{\rm sw} = 8$  kHz. The bandwidth of the phase-locked loop (PLL) is set to 2 Hz.

Fig. 2 shows a map of the grid inductance values for which the system turns unstable as a function of the pole parameters  $\zeta$  and  $\beta_c$ . Two highly robust regions can be observed around the points  $(0.05, 3.5\alpha_c)$  and  $(0.1, 0.1\alpha_c)$ . In the following, an example tuning based on the choice  $\alpha_c = 2\pi \cdot 400$  rad/s (8 p.u.),  $\zeta = 0.15$ , and  $\beta_c = 4\alpha_c$  is employed. A deliberate choice of avoiding the regions of high robustness in Fig. 2 is made in order to maintain satisfactory dynamic performance, while still achieving stable operation for grid inductances corresponding to a SCR of unity.

This example design is then compared to a direct pole placement design presented in [5] and an LQR-based indirect





Fig. 4. Experimental results under nominal conditions ( $L_{\rm g} = 0$ , SCR = 8) of the proposed design, a reference direct design, [5], and a reference indirect design [8]. (a) Positive-sequence reference tracking (b) Negative-sequence reference tracking (c) Symmetric grid-voltage dip of 0.5 p.u. (d) Asymmetric grid-voltage dip corresponding to a single line-to-ground fault behind a transformer.

pole placement design presented in [8] that extends on the work in [26]. For the direct design, the bandwidth of the dominant pole is selected as  $\alpha_c = 8$  p.u. to obtain identical reference-tracking characteristics under nominal conditions. For the indirect design based on LQR, the weights are selected

Fig. 5. Experimental results under weak grid conditions ( $L_{\rm g}=0.92$  p.u., SCR = 0.96) of the proposed design and a reference indirect design [8]. (a) Positive-sequence reference tracking (b) Negative-sequence reference tracking (c) Symmetric grid-voltage dip of 0.5 p.u. (d) Asymmetric grid-voltage dip corresponding to a single line-to-ground fault behind a transformer.

as Q = diag[35, 0, 30, 15] and R = 1. Fig. 3 shows the pole maps for these three designs for grid inductance values ranging from 0 p.u. to 1 p.u. The direct design [5] becomes unstable already for grid inductance of 0.27 p.u., whereas the proposed and the indirect design [8] remain stable for the range of examined grid inductances.

To demonstrate the performance of the proposed pole placement design, a set of experiments are presented in Figs. 4 and 5 for grid inductance values of 0 p.u. (SCR = 8) and 0.92 p.u. (SCR = 0.96), respectively. The direct design [5] is omitted from Fig. 5, since it is unstable. Both figures comprise positive- and negative-sequence reference tracking in subfigures (a) and (b), respectively, and both symmetric and asymmetric grid-voltage dip in subfigures (c) and (d), respectively. While the reference-tracking performance of all designs can be observed comparable under nominal conditions, the proposed design has better dynamic performance under weak grid, cf. Figs 5(a) and 5(b), as compared to the indirect design [8]. The responses to symmetric and asymmetric gridvoltage dips are also comparable under nominal conditions. Furthermore, complete cancellation of the negative-sequence disturbance in the current is achieved irrespective of the grid inductance. However, a slowly oscillating mode with low amplitude can be observed in the response of the proposed design to an asymmetric grid dip. This mode is caused by the partial pole-zero cancellation of the negative-sequence integrator pole in the output admittance, and its characteristics depend on the choice of the damping ratio  $\zeta$ . Under weak grid conditions, the proposed design exhibits better symmetric and asymmetric disturbance rejection as compared to the indirect design [8].

# V. CONCLUSION

This paper presented an enhanced direct pole placement design for positive- and negative-sequence current control of grid converters. The pole placement design was synthesized from the existing body of literature on multi-frequency current control. The resulting design is robust to grid inductance variations and achieves comparable dynamic performance relative to existing state-of-the-art pole placement designs under nominal strong grid conditions. Furthermore, the proposed design is simpler than the existing robust pole placement designs, while providing good dynamic performance under weak grid conditions.

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