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A Transmitter IC with Supply Tuning for Frequency-Reconfigurable Antenna Cluster

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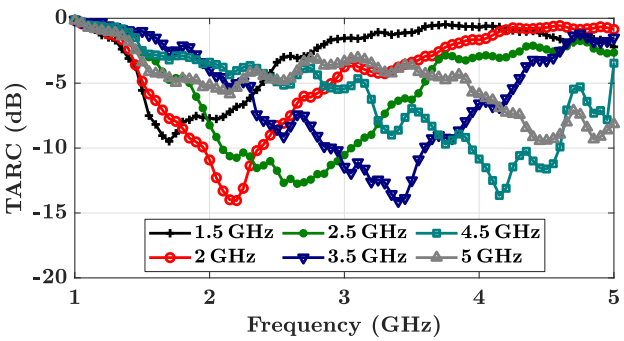
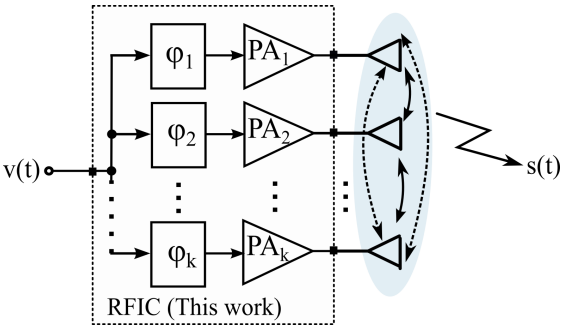
***Abstract*— Active reconfiguring of the frequency response of an antenna cluster was recently demonstrated involving an integrated transmitter and antenna cluster. The tuning method solely relies on scaling the antenna cluster feed amplitudes and phases, and entirely eliminates the typically required on-chip or off-chip matching networks. This work now advances the prior art by demonstrating and presenting improved solutions for on-chip amplitude and phase scaling blocks. In this paper, we present an optimization for phase resolution, resulting in 5 bit phase tuning architecture. Furthermore, we present an analysis of amplitude tuning on the efficiency and impedance variation for antenna cluster feeds. Two different amplitude scaling alternatives are considered: formerly studied switched capacitor power amplifier (SCPA) topology and a new low-dropout-regulator (LDO) based supply scaling of the class-D power amplifier. The designs are simulated in a 28-nm bulk CMOS technology at 1.5 GHz and 5 GHz respectively. The simulation results indicate that the LDO-based supply tuning method is superior to SCPA in terms of variation on efficiency and output impedance over the amplitude tuning code. The proposed circuit provides 15 dB amplitude tuning range with a 54 Ω impedance interface and 48% drain efficiency at 1.5 GHz whereas it provides an impedance interface of 84 Ω with 23% drain efficiency at 5 GHz.**

I. Introduction

Next generation wireless devices are heading for higher data rates and multiband communication. Recently, a frequency tunable antenna concept known as antenna cluster tuning was proposed [1], which enables agile frequency-reconfigurable operation of the antenna. The method eliminates the need of traditional on-chip/off-chip matching components. Though it may resemble beamforming techniques, it alters only the frequency response of the antenna rather than steering the beam or adjusting the polarization. Antenna cluster tuning concept was verified with transmission line based power dividers and phase shifters at two frequencies 2 GHz and 4.3 GHz [3], whereas a radio frequency integrated transmitter circuit (RFIC) demonstration [2] provides robust tuning across a wide band as illustrated in Fig. 1. Although the on-chip amplitude and phase scaling circuits provide sufficient amplitude and phase tuning range in order to tune the antenna cluster, the RFIC outputs suffer from the phenomenon that the optimal load impedance depends on the output amplitude level [2],[4]. This affects the output power and efficiency of the driving stage. In this paper, we are addressing the aforementioned issues with suitable solutions resulting in optimized phase tuning architecture along with the analysis on amplitude tuning for improved efficiency and optimal impedance at the antenna cluster feeds. Section II presents the system level diagram of the integrated transmitter circuit, and the subsections describe the optimized designs for phase- and amplitude tuning blocks. Two different alternatives are examined for amplitude scaling with main focus on reducing the impedance variation at the antenna cluster feeds. Section III discusses the simulation results of two alternative methods, and shows that the proposed method outperforms the prior approach. Finally, the conclusions are given in Section IV along with further directions.



(a)



(b)

Fig. 1. (a) Measured antenna cluster tuning performance demonstrated in [2] with an integrated transmitter, and represented in terms of tuning benchmark total active reflection coefficient (TARC) (b) Integrated transmitter with weighted signal generation comprising of phase tuning blocks $\varphi_1 - \varphi_k$ and amplitude tuning blocks $PA_1 - PA_k$. The input RF signal $v(t)$ drives each tuning branch ie. (φ_k, PA_k), and accordingly tunes the kth antenna element along with transmission signal $s(t)$.

II. Transmitter Architecture

The transmitter architecture consists of k tuning branches for associated k element antenna cluster and an input buffer.

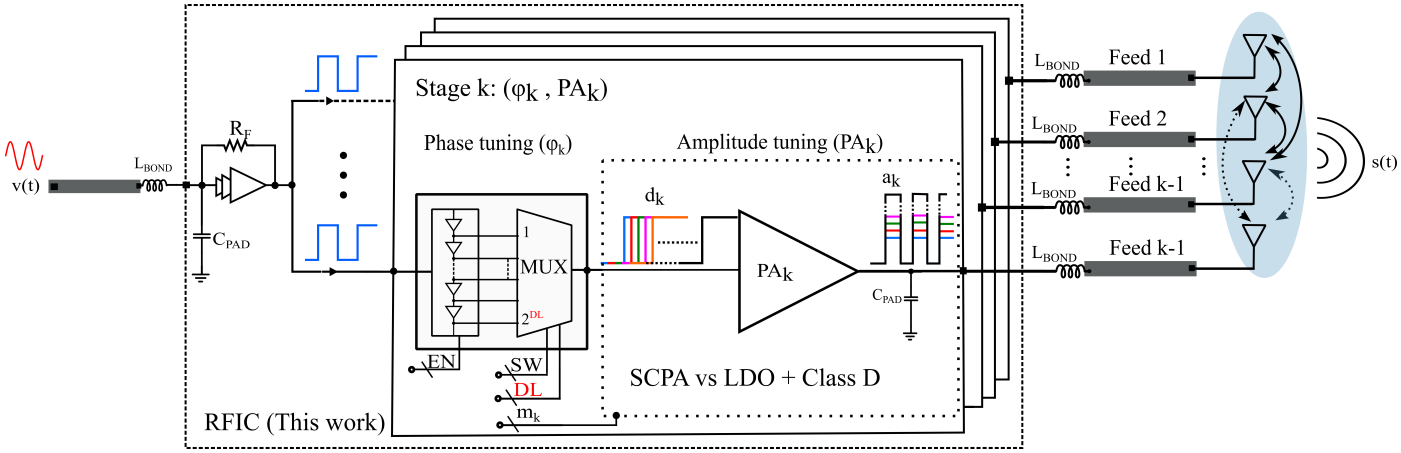
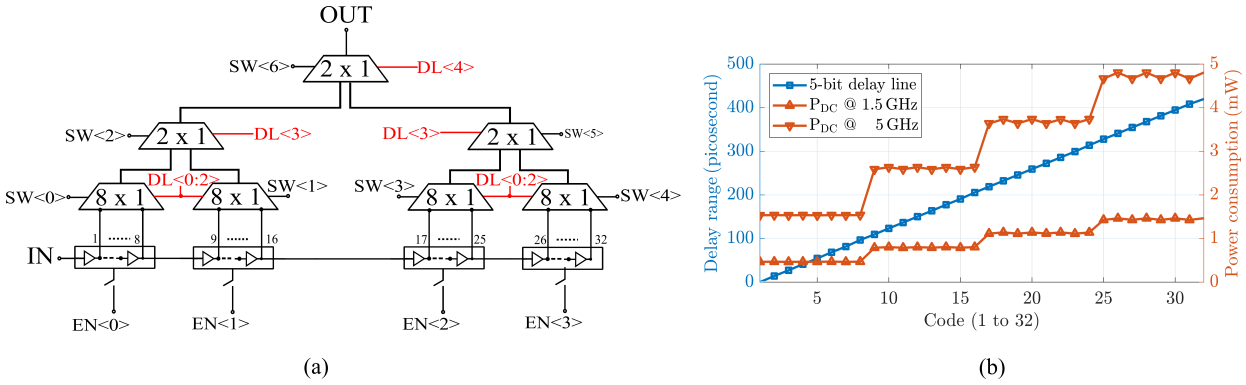


Fig. 2. Block diagram of the integrated transmitter circuit with k-tuning stages driving a k-element antenna cluster. In this case ($k = 4$), the input signal $v(t)$ is fed to each tuning branch consisting of the phase tuning block φ_k with $DL = 5$-bit resolution, followed by an amplitude tuning block PA_k of resolution $m_k = 4$ respectively. The amplitude scaling is demonstrated with two alternative solutions: the switched capacitor power amplifier (SCPA) and a low dropout regulator based supply scaling of the class-D power amplifier.



(a) (b)

Fig. 3. (a) Optimized phase tuning architecture (b) An optimized 5-bit delay line characteristics vs phase scaling codes.

Fig. 2 illustrates the system block diagram where the input buffer transforms and distributes the input signal $v(t)$ to RF pulses in the range of 1.5 GHz to 5 GHz. It also drives each tuning slice consisting of a phase tuning block φ_i and amplitude tuning block PA_i where $i = 1 \ldots k$. Table 1 shows the required amplitude and phase (delay) specifications for the antenna cluster utilized in [2]. For antenna cluster tuning, these specifications pour down to roughly 16.5 dB amplitude range and 405 ps delay tuning range. These specifications pave our way to the design optimization and alternative solutions discussed in the following subsections with necessary circuit level details.

A. *Delay tuning block*

The CMOS delay lines have been recently emerged and can be utilized for delay tuning capabilities [5]. Here, the delay tuning block φ_k consists of a tapped delay line and a multiplexer as an auxiliary block as shown in Fig. 2. The required phase tuning block delay range is now 405 ps (previously 860 ps) based on the requirements mentioned in Table 1. This enable us to downsize the design to delay resolution of $DL = 5$-bit (previously 6-bit) as illustrated in Fig. 3 (a). The criterion for the reduction is based on selection

Table 1. Relative weighted amplitudes (dB) and delay specifications (ps)

Freq. (GHz)	a_1	a_2	a_3	a_4	d_1	d_2	d_3	d_4
1.5	0	-28*	-5.3	-14.8	405	580*	297	338
2	-1.3	-22*	0	-6	256	27	135	175
2.5	-7.8	-16	0	-2	189	54	27	54
3	-15.2	-11.7	-3.1	0	459	391	324	337
3.5	-16.5	-9.7	-7.3	0	364	337	229	243
4	-10.3	-6.5	-9.3	0	310	310	175	175
4.5	-3.9	-3.2	-8.2	0	283	270	135	121
5	0	-3.3	-4.7	-3.7	243	243	81	67
Range	16.5	16	9.3	14.8	405	391	324	338

* Feeds with smaller contribution has minor effect on the antenna cluster tuning, and these feeds can be considered in an off state.

of the dominant feeds whose phase accuracy matters the most for antenna cluster tuning.

Regarding improvements, the delay line is divided into four subsections and each subsection incorporates an enable control $EN < 0 : 3 >$. Based on the phase scaling code $DL < 0 : 4 >$, the switch control $EN < 0 : 3 >$ first select respective delay sections, and afterwards the multiplexer branch is selected with additional control $SW < 0 : 6 >$.

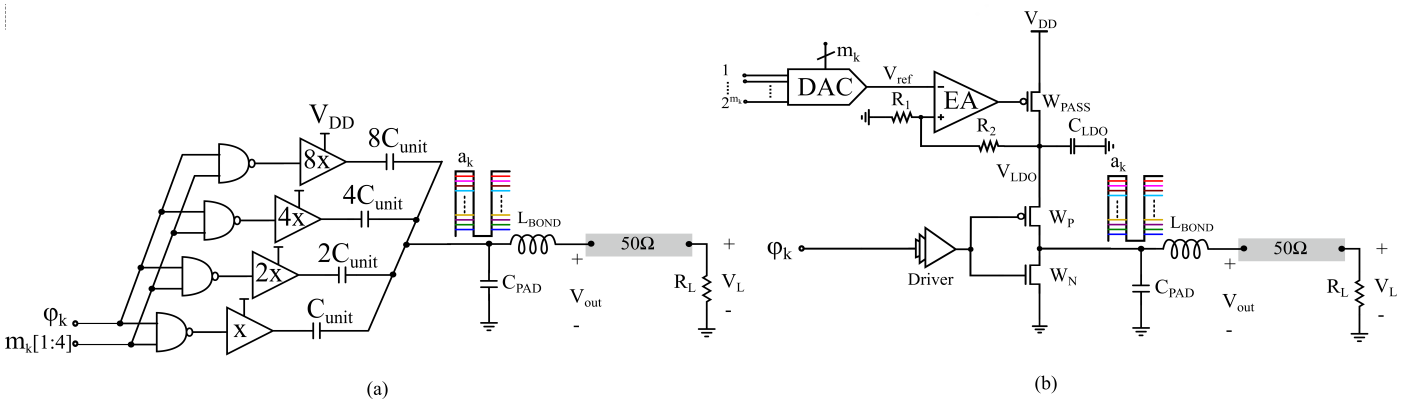


Fig. 4. (a) A 4-bit binary weighted SCPA structure with class-D PA units (b) A LDO based supply scaling topology for class-D PA

In this way, we are able to produce 32 delayed versions d_k of an RF pulse signal with a 5-bit delay line as illustrated in Fig. 3 (b). The simulations are performed at the spectrum boundaries, i.e., 1.5 GHz and 5 GHz respectively. The results show that the circuit provides sufficient delay tuning range of 420 ps with 13.2 ps resolution.

B. Amplitude tuning block

The amplitude tuning block PA_k has three main tasks: Firstly, it scales the amplitude of the antenna cluster feeds. Secondly, it needs to drive the antenna cluster with sufficient output power. Thirdly, the transmitter outputs must maintain a constant impedance interface so that the maximum power can be transferred to each antenna feed. Finally, it needs to abide by the constraint that the above mentioned tasks are achieved in absence of a matching network at the output of PA_k. In order to fulfill these targets, two techniques are studied and examined as followed in terms of performance metrics such as the required amplitude scaling range, impedance variation and efficiency of the PA_k block.

1) Switched capacitor power amplifier

Switched capacitor power amplifier (SCPA) has recently stood up as an efficient digitally controlled PA topology [6]. The design choice is based on technology scaling, high efficiency and rail-to-rail signaling. It typically contains multiple switch-mode PAs in parallel, such as class-D or class-G, acting as a driving source for the output capacitor array. The capacitances driven ON/OFF are $C_{ON} = (n/N)\,C$ and $C_{OFF} = \left(\frac{N-n}{N}\right)C$ where $n = 1 \ldots N$ and C represents the total capacitance of the array. As a result, a capacitance-ratio dependent voltage division occurs at the output node give by $V_{out}(t) = V_{DD}\left(\frac{C_{ON}}{C}\right) = V_{DD}\left(\frac{C_{ON}}{C_{ON}+C_{OFF}}\right)$. In this work ($N = 4$), a 4-bit SCPA topology with binary weighted class-D PA units $x - 8x$ has been designed as illustrated in Fig. 4 (a). The fundamental output power P_{out} scales depending on active PA units (n) which can be given by Eq. (1). This points out another important factor which is the turn-on resistance Z_{on} of the PA devices, and can be expressed by $Z_{on} = 1/[\frac{kW}{L}(V_{DD} - V_G - |V_{th}|)]$. Using a sub-micron technology with a given supply voltage V_{DD} and threshold voltage V_{th}, the resistance Z_{on} depends on the PA device size (W). It contains two interdependent parameters, i.e., the number of active PA units n and their associated resistance Z_{on}. As a result, the resistance Z_{on} varies with the number of active PA units n or indirectly with the amplitude scaling code $m_{\mathbf{k}}$. Therefore, another alternative solution is indispensable so that the PA_k output can offer code independent impedance interface along with desired amplitude scaling.

$$P_{out} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2\left[\frac{VDD^2}{R_L\left(1+\frac{Z_{on}}{R_L}\right)}\right] \tag{1}$$

2) Low dropout regulator supply scaling

Advancing our design approach based on the turn-on resistance Z_{on}, we have a liberty to scale the supply V_{DD} of a PA for a given device size, i.e., $Z_{on} = 1/[\frac{kW}{L}(V_{DD} - V_G - |V_{th}|)]$. In order to scale the supply, the low dropout regulator (LDO) technique [2] has been presented where the LDO output scales the supply of a single switch mode PA such as class-D power amplifier. In comparison to [2], this work describes the amplitude tuning block specifications in terms of output power, efficiency and turn-on resistance of the class-D PA along with the amplitude tuning range.

Fig. 4 (b) shows the schematic of the design where the input phase tuning signal φ_k is taken as an input to the amplitude tuning stage PA_k. The supply scaling feature is achieved with an LDO and digital to analog converter (DAC). The DAC resolution $m_k = 4$ is decided to generate 16 different reference voltage levels V_{ref}. Assuming the error amplifier (EA) gain is high, and drives a large pass device W_{PASS}, the LDO output voltage can be given by $V_{LDO} = (1 + R_1/R_2)V_{ref}$ This describes the supply scaling feature of the LDO and accordingly regulates the PA supply along with scaled output. Regarding output power, the PA device sizes W_P and W_N comes into play while acting as a switch with turn-on resistance $Z_{on} = 1/[\frac{kW}{L}(V_{LDO} - V_G - |V_{th}|)]$. Besides amplitude scaling, one can notice that the effect of V_{LDO} on the output signal and Z_{on}. Assuming that

the V_{LDO} lies in linear region, this reflects in a linearly scaled amplitude a_k along with less variant Z_{on} for certain device sizes (W_P, W_N). As a consequence, this approach enables amplitude scaling, and also provide a relatively constant impedance interface in comparison to the SCPA method where Z_{on} is dependent on the amplitude scaling code m_{k}.

III. Simulation Results and Discussion

The on-chip delay tuning and amplitude tuning blocks are designed for the 28-nm CMOS technology. The delay generation feature utilizes inverter-based buffers with delay resolution of 13.5 ps. For a 5-bit design, the delay line achieves delay range of 420 ps that is sufficient for the antenna cluster under consideration.

A 4-bit SCPA structure is simulated with supply voltage of 1.8 V and drives the capacitor array with $C_{\mathrm{unit}} = 1\,pF$. The phase tuned signal φ_k is applied to selective PA unit with ideal 0.9 V to 1.8 V level shifter and driver. This is intentionally done in order to properly rectify the performance metrics such as SCPA efficiency and interface impedance Z_{on}. One notable point is that the typical bandpass matching network is excluded as required by the antenna tuning method. Regarding the low dropout regulator method, the LDO utilizes 2.5 V supply as an input where as the resistive DAC uses 0.9 V as a reference in order to generate 16 different reference voltages. With similar feedback resistors $R_1 = R_2 = 10\,k\Omega$, enable us to scale the LDO output voltage $0.6\,V \leq V_{LDO} \leq 1.8\,V$. For a fair comparison of two approaches, the amplitude scaling range and the PA device sizes are chosen to be roughly in the ball park.

It is clear that the SCPA method provides a larger amplitude range of nearly 25 dB whereas the LDO technique enables 12 to 15 dB range across the spectrum as illustrated in Fig. 5 (a). Both approaches feature maximum output power of 11 to 12 dBm for each amplitude tuning block. For smaller values of m_k, the SCPA activates PA units with large turn-on resistances, and causes smaller PA devices to contribute towards the amplitude scaling. In fact, the impedance variation is drastic across low and high amplitude scaling codes. On contrary, the LDO method results in a region where Z_{on} reaches a constant value of 54 ohm at 1.5 GHz while the 5 GHz case features an impedance of 84 ohm. The efficiency of the SCPA topology has also a scaled behaviour, while the LDO topology features nearly constant 23% to 48% efficiency, as illustrated in Fig. 5 (c). Hence, this study indicates that the LDO based supply tuning enables required amplitude scaling capability with code independent impedance interface and constant drain efficiency across the spectrum.

IV. Conclusions

The transmitter IC features a wideband transmitter front end for antenna cluster tuning. The design optimization of phase tuning block results in desired functionality with 420 ps delay range and reduced power consumption. The amplitude scaling has been examined with two different alternatives, i.e., the SCPA and LDO based supply scaling method. Although,

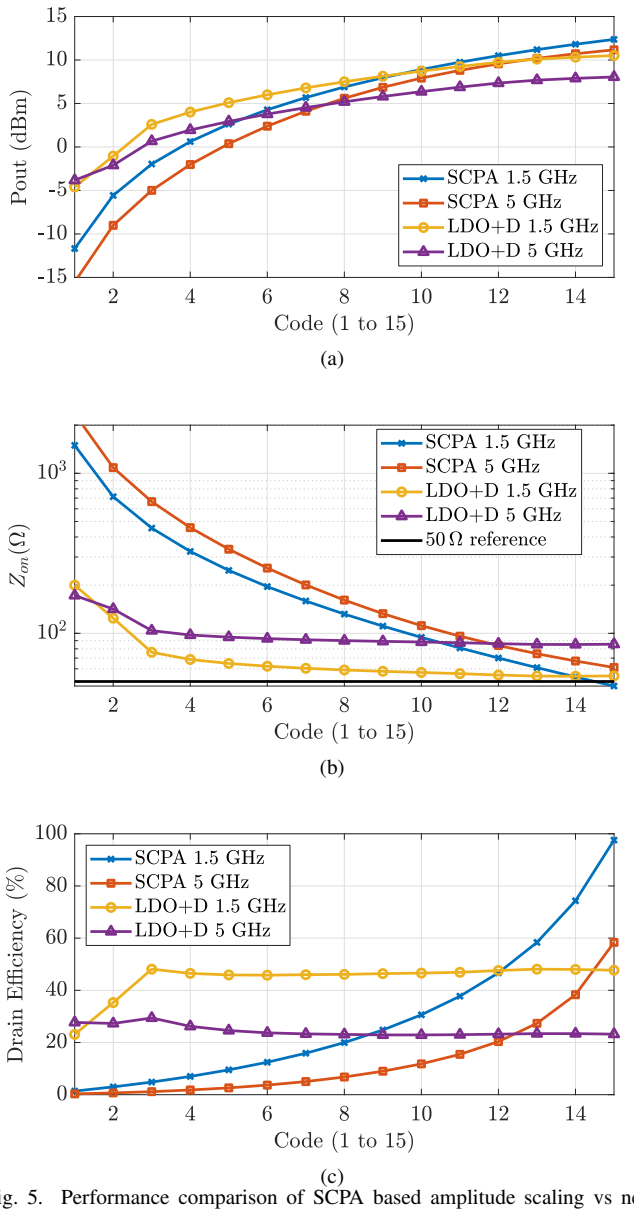


Fig. 5. Performance comparison of SCPA based amplitude scaling vs new method for 1.5 GHz and 5 GHz (a) Impedance Z_{on} profile (b) Output power (c) Drain efficiency

the SCPA provides large scaling range it suffers from the impedance variation phenomenon owing to amplitude scaling. In contrast, the proposed LDO based method offers sufficient amplitude range and constant impedance interface of 54 ohm to 84 ohm to the antenna cluster for majority of the codes. The proposed LDO based method provides code-independent impedance interface at the RFIC outputs, an essential feature to tune the frequency reconfigurable antenna clusters. Meanwhile, it delivers maximum output power of 8 to 12 dBm and amplitude scaling range of 13 to 15 dB with drain efficiency ranging from 23% to 48% for each antenna element across the spectrum.

REFERENCES

[1] J.-M. Hannula, J. Holopainen, and V. Viikari, "Concept for frequency-reconfigurable antenna based on distributed transceivers," *IEEE Antennas and Wireless Propagation Letters*, vol. 16, pp. 764–767, 2017.

[2] A. R. Saleem, K. Stadius, J. M. Hannula, A. Lehtovuori, M. Kosunen, V. Viikari, and J. Ryynänen, "A 1.5–5-GHz integrated RF transmitter front end for active matching of an antenna cluster," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 11, pp. 4728–4739, 2020.

[3] J.-M. Hannula, T. Saarinen, J. Holopainen, and V. Viikari, "Frequency reconfigurable multiband handset antenna based on a multichannel transceiver," *IEEE Transactions on Antennas and Propagation*, vol. 65, no. 9, pp. 4452–4460, Sep. 2017.

[4] A. R. Saleem, R. Luomaniemi, A. Lehtovuori, K. Stadius, M. Kosunen, V. Viikari, and J. Ryynänen, "A frequency tunable mimo antenna cluster with transmitter ic," in *2021 15th European Conference on Antennas and Propagation (EuCAP)*, 2021, pp. 1–5.

[5] J. Lemberg, M. Martelius, E. Roverato, Y. Antonov, T. Nieminen, K. Stadius, L. Anttila, M. Valkama, M. Kosunen, and J. Ryynänen, "A 1.5–1.9-GHz all-digital tri-phasing transmitter with an integrated multilevel class-D power amplifier achieving 100-MHz RF bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 6, pp. 1517–1527, 2019.

[6] J. S. Walling, "The Switched-Capcitor Power Amplifier: A Key Enabler for Future Communications Systems," in *2019 IEEE 45th European Solid State Circuits Conference - (ESSCIRC)*, Feb 2019, pp. 174–176.