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Published in:
ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference, Proceedings

DOI:
10.1109/ESSCIRC53450.2021.9567865

Published: 13/09/2021

Document Version
Peer-reviewed accepted author manuscript, also known as Final accepted manuscript or Post-print

Please cite the original version:
Akbar, R., Shaheen, R. A., Rahkonen, T., Tze, C., Stadius, K., & Parssinen, A. (2021). A 38.5-to-60.5 GHz LNA with Wideband Combiner Supporting Cartesian Beamforming Architecture. In *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference, Proceedings* (pp. 199-202). IEEE.
https://doi.org/10.1109/ESSCIRC53450.2021.9567865

A 38.5-to-60.5 GHz LNA with Wideband Combiner Supporting Cartesian Beamforming Architecture

Rehman Akbar[*1], Rana A. Shaheen[*1], Timo Rahkonen[#2], Cheung Tze[¤3], Kari Stadius[¤3], Aarno Pärssinen[*1]
[*]*Center for Wireless Communications, University of Oulu*, Finland
[#]*Circuits and systems Group, University of Oulu*, Finland
[¤]*Aalto University* , Finland

***Abstract*—Current millimetre-wave (mmW) 5G NR standard supports multiple bands at 24.5/28/37/39/43/47GHz for communications. To cover several bands of the 5G NR and reaching lower end of unlicensed 60GHz band for 802.11ad, this work presents a wideband phased array front-end with LNA and two VGAs for scalar-only weighting function, and a wideband combining network of each signal weight in mmW domain for beamforming. In this work, two array elements are combined in two cascaded stages for extremely wideband operation. Combined load resonances are distributed and adjusted appropriately in each of the combining stages to achieve a flat response over the band of 38.5-60.5GHz. A single array path achieves rms gain of 8.5-12.5dB, noise figure of 6.2-8.1dB, and IP1dB of -33 to -26dBm. The measurements show ≈ 6dB of array gain when the two phased array elements are combined in phase with +0.6dB to -0.4dB maximum gain error in the mmW VGAs. The prototype is implemented using 28nm CMOS.**

***Index Terms*—5G, millimetre-wave, wideband, LNA, VGA, wideband mmW-combining, Cartesian beamforming Architecture**

I. Introduction

Future 5G user equipment (UE) requires multi-band operation to support high speed multi-standard communication. Millimetre wave (mmW) 5G new radio (5G NR) standardized by 3GPP has already allocated multiple frequency bands from 24.5 to 29.5GHz, 37, 39 and 47GHz frequency ranges. To cover multiple channels and over broad range of bands in mmW 5G systems, the development of a wideband front-end is required. This avoids parasitics coming from the mmW band selection switches and allows to receive multiple channels in parallel. Different bands and channels can be then separated in the IF domain [1]. In recent studies, wideband front-ends focus only on LNAs [2]–[4] and VGAs [5], [6]. Those are omitting one of the major challenges of wideband signal combining at very broad frequency range. Recent work provides narrow-band solutions like [7] in vector modulator-based phase shifting, or up to 18% in cartesian combining [8]. If a large bandwidth of 50% or above is needed as shown in LNA's of [3] and [4] and VGA's [5], [6], the combining network bandwidth also becomes critical.

This work is targeted for cartesian combining architecture as in [8] for wideband beamforming front-end. Core element of the architecture is the wideband front-end with mmW signal combiner. Chip incorporates two LNAs with fine step gain control per antenna that are individually combined. The gain steps will support vector modulator with 24-by-24 constellation with 4.5bit resolution.The circuit uses two main methods to achieve broadband response. First, the phase shift needed for beamforming is distributed between mmw and IF domains, and quadrature combining is moved to IF-to-BB down-conversion using quadrature LO at IF [9]. To reduce the number of down conversions, the scalar only real and imaginary weights are combined before the down-conversion in Fig.1. It avoids the generation of 90° phase shift for base vectors over a broad range of frequencies in multi-band receiver that requires additional calibration due to phase and amplitude inaccuracies in the LO [8]. Second, most stage-to-stage couplings employ the idea of double-resonant transformer coupling: with loose enough coupling in the transformer, primary and secondary can be tuned to different resonance frequencies, and together they peak up the corners of the band.

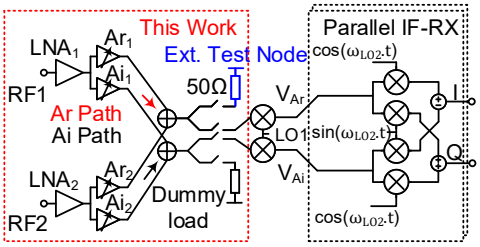

Fig. 1: Proposed wideband beamforming architecture. In this work, two element wideband mmW combiner is implemented and characterized through external test node

Two wideband LNAs and the combining front-end is characterized through an external test port shown in Fig. 1. Section II describes design methodology of the wideband LNA followed by VGA and wideband combiner design aspects, respectively. Measurement results are presented in section III. Section IV concludes the work.

II. Circuit Design

A. Low Noise Amplifier

LNA is composed of three cascaded stages and each stage utilizes a transformer-based passive load. The implementation of LNA is shown in Fig. 2. Each LNA stage utilizes active devices that are connected in common source configuration for improved inter-stage matching conditions. Common source inductive degeneration is utilized to match the input impedance simultaneously for optimum noise and gain. Maximum bandwidth of the input matching circuit is mainly limited by the

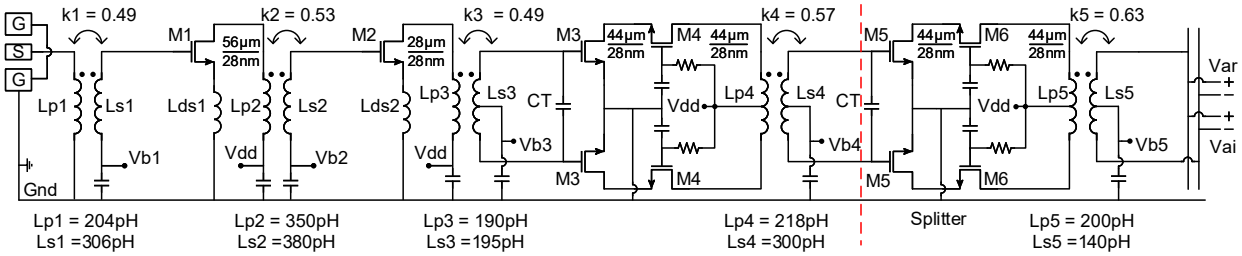

Fig. 2: Three stages of wideband LNA and fourth stage is used to split signal for VGAs named Ar and Ai

parasitic capacitance of the input pad. The simulated model of the pad is shown in Fig. 3 and has a simulated capacitance of $35fF$.

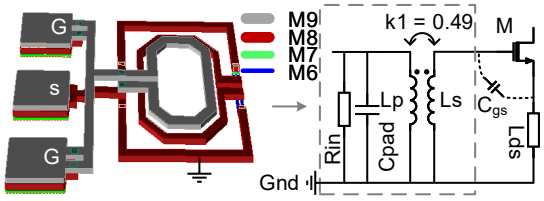

Fig. 3: 3D layout of mmW input pad and first transformer and input matching network with pad capacitance

In order to cover wider bandwidth, multiple-order LC matching network is inevitable, for example, using transformers [3], [4]. Transformers offer compact implementation and more degrees of freedom for controlling the operational bandwidth. The control is achieved by the tuning of the coupling between the primary and secondary inductors [4]. A simple transformer-based resonator generates two resonance frequencies, and component values can be defined as,

$$f_L = \frac{1}{2\pi\sqrt{LC(1+|k|)}}, f_H = \frac{1}{2\pi\sqrt{LC(1-|k|)}} \quad (1)$$

$$|k| = \frac{f_H^2 - f_L^2}{f_H^2 + f_L^2} \quad (2)$$

where f_L and f_H are the frequencies of the low and high resonances to be generated by the circuit model in Fig. 3, and k is the coupling factor. To cover the desired bandwidth for noise matching, coupling factor is set to 0.49 in such a way that f_L and f_H are at 26GHz and 65GHz, respectively. A single stage NMOS transistor instead of a cascode design is used in the first two stages of the LNA to minimize the output parasitic capacitance. The first stage transistor size is optimized for matching and it's biasing is selected having high enough unity gain bandwidth (fmax), such that the first stage provides sufficiently flat gain for the whole bandwidth.

Similar to the input stage, the inter-stage matching of the LNA is achieved with transformers. The inter-stage transformers also act as load resonators with carefully selected resonance frequencies (Fig. 2). Resonance frequencies of the following stages (resonators) are adjusted in a way that they compensate the gain drop from the previous stages. Accumulated frequency response from each stage obtains reasonably flat gain response as will be seen in the following simulations and measurements.

B. mmW VGA Design

VGAs provide the scalar weighted sums for beamforming. The splitter shown in Fig. 2 drives two VGAs (real (Ar) and imaginary (Ai) amplifiers). The VGA unit Gm-cell is shown in Fig. 4. The unit Gm-cell of the VGA contains dummy block to keep constant capacitance at the LNA output and negative-Gm block to keep output resistance constant across all VGA settings in order to reduce the gain and phase variation [7], [8]. The paracistics extraction of VGA is done at two levels. First, each unit cell is RC-extracted. Second, interconnects between unit cells are extracted with 2.5D EM simulator. After layout optimization, VGA still has large wiring parasitics at the output side. It defines the higher side corner frequency of the circuit. A trade-off is made between the number of GM-cell units, corner frequency and phase accuracy in the beamforming. Therefore, VGA weighting scheme is modified from 1x, 2x, 4x and 8x bits to 1x, 2x, 3x and 6x which makes each VGA is effectively 4.5bits. The modified weighting scheme reduces the phase accuracy of the outer circle of phase shifter constellation from 3.75° to 5.6°.

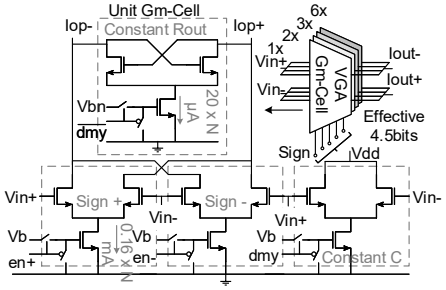

Fig. 4: VGA Gm unit cell with constant-C and constant-Rout blocks.

C. mmW wideband combiner

Here, a two-stage active combiner concept similar to [8] is utilized, as illustrated in Fig.5. First, the VGA with large output capacitance is first coupled to a buffer. Actual combining is done by combining two real and imaginary sums in stage1, and then to two other LNA outputs in stage 2. The circuit is measured with GSG probe from a test port available at stage 1. Transformer-based resonant loads of these combiners are designed so that their resonances are distributed and compensate each others and LNA's response. Transformer coupling coefficients of 0.4 and 0.5 were used to distribute the input and output side resonances. Fig. 6 shows the simulated response of a single element (LNA, VGA and stage 1 combiner) has gain of more than 16dB from 35 to 63GHz. The Gm-ar in

stage 2 combiner drives 50Ω external load and has loss of 6dB. The 6dB loss to 50Ω external node is due to high output impedance of driving Gm stage approximately 4 times the load impedance. The proper impedance transformation with good output matching required additional passives for matching [5]. However, due to area limitation only single transformer was utilized to keep wideband frequency response at the output.

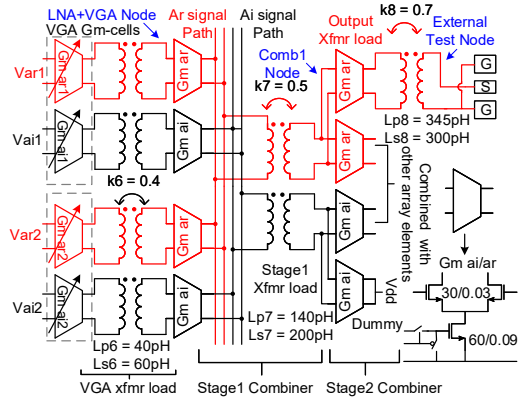

Fig. 5: Combining network of two phased array elements with external test node for characterization of LNAs and combining network for Ar signal path only.

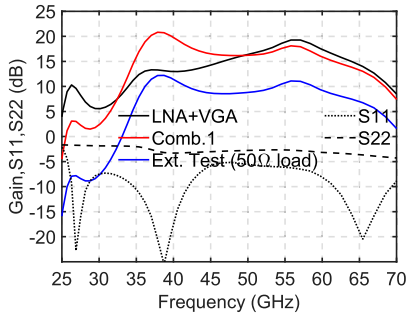

Fig. 6: Simulated response of the single element at the output of the VGA, after on-chip combining node (comb1) and at 50Ω external test node.

III. Measurements

The wideband front-end was implemented using 28nm bulk-CMOS process. Microphotograph is shown in Fig. 7. The front-end response was measured through a single-ended test port placed on the top side of the otherwise symmetrical elements. A single LNA consumes 39mA, single VGA 4.5mA and a single Gm-stage in combining network consumes 5mA from 0.9V supply.

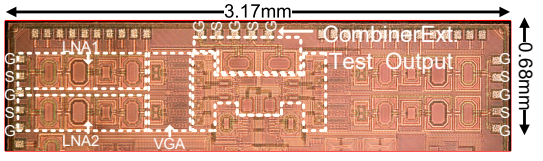

Fig. 7: Chip containing 4 phased array elements. 2 elements on left side and 2 on right and combined in the middle. Only left side LNAs are measured through external test node. Active area of one LNA $0.25 \times 0.7mm^2$, VGA $(4 \times (0.14 \times 0.063))mm^2$, Combiner $0.4 \times 0.78mm^2$

Measurements show the expected frequency response shown in Fig. 8. However, there is up to ±1dB variation between Ar1 and Ar2 responses to output, and ±1dB w.r.t rms gain, when e.g. Ar1 polarity is switched inside the path, as shown in Fig. 9(a). The elements themselves are very symmetrical and vertically flipped. The single-ended test port is on the top side nearest to Ar stage 1 combiner. Generally, the transformers should have very good isolation from each other. However, it was found in post-layout (post fabrication) EM simulations of the entire metallization that there are different values of coupling appear from the Ar combining transformers to the test output balun transformer, i.e. −18dB for plus sign and −15dB for minus. This is potentially the main reason for the difference in the two responses. Within the frequency range of 38.5 to 60.5GHz, the rms gain of measured curves ranged from 8.5 to 12.5 dB, with input matching below -8dB.

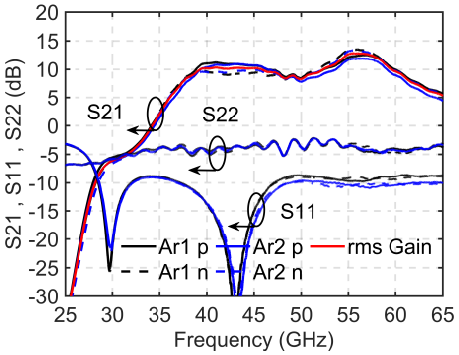

Fig. 8: Measured wideband response of element 1 and 2. VGAs set to maximum with positive and negative signs.

The combining of signals with plus sign of Ar1 and Ar2 VGA and cancellation of signals with plus sign of Ar1 and minus sign of Ar2 is shown in Fig.10. The measurements are done by feeding two in-phase signals through GSGSG differential probes and then measuring combined single-ended output. For combining Ar2 is swept for all gain control words and kept Ar1 to maximum. The -3dB bandwidth of front-end is defined from the maximum combining gain curve in Fig. 10, using maximum gain as a reference at 56 GHz. Due to error in flatness of combined gain response, the bandwidth is divided into two sections, 38.5 to 48GHz and then 50.5 to 60.5GHz, resulting a 19.5GHz -3dB bandwidth. Fig. 9(b) shows combining gain error w.r.t ideal 6dB combining gain and Fig. 9(d) the VGA gain error for all gain control words. Error is within -0.4 to $+0.6$dB over the frequency range. The rms phase error of the combined signal is 0.1° to $+5.4^\circ$ across the whole band (shown in Fig.9(c)).

The noise figure (NF) is measured from 30GHz to 50GHz due to frequency limitation of the available noise source. In Fig. 11(a), minimum measured NF is 6.2dB at 45GHz increasing to 7.5dB at 50GHz. It follows the simulation at higher side of spectrum. The NF above 50GHz can be estimated with simulations, showing 8.1dB NF at 61GHz. Fig. 11 (b) shows the input referred compression point (IP1dB) of a single element ranging from -33 to -26dBm over the band. Performance comparison of the front-end with the existing state-of-the-art (SoA) LNAs and VGAs is presented in Table 1. Due to lack of other very wideband combiners in the

literature, this work (LNAs + VGAs + Combiners) is compared with wideband LNAs and VGAs. This work has comparable NF, Gain, Bandwidth and phase variation with the other SoA designs with similar LNA and VGA power consumption, and in addition can provide combined output from multiple antennas over the same frequency range.

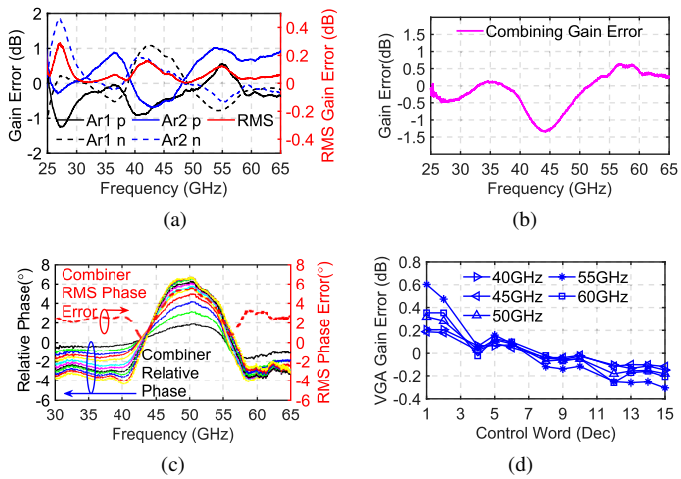

Fig. 9: Error: (a) Gain error between elements w.r.t to rms gain; (b) Combining gain error w.r.t 6dB ideal combining;(c) Combining Phase error; (d) VGA step gain error

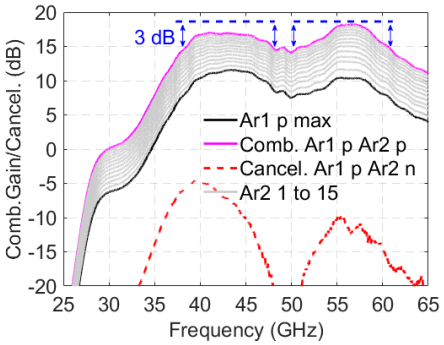

Fig. 10: Measured combined gain of element1 and element2 VGA Ar1 is fixed and VGA Ar2 sweeps from 1 to 15.

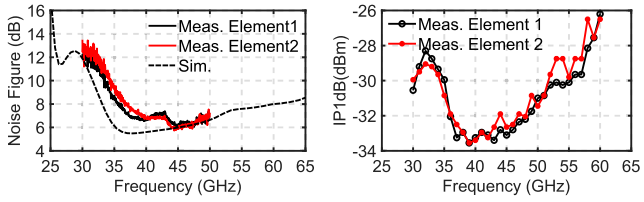

Fig. 11: (a) Measured noise figure of single element (b) measured input referred compression point (IP1dB) of element1 and element2

IV. Conclusion

This paper demonstrates 38.5-60.5GHz front-end for beamforming receivers targeted to cartesian weighted phased arrays. Wideband combining network adapts distributed resonances in multiple combining stages to maintain the wideband response. The gain error of VGAs is within $+0.6$ to -0.4dB over the entire bandwidth. The fine-tuned 90° phase shift for cartesian combining and additional gain can be provided at the IF stage, where multiple frequency bands and channels can be further separated and processed. Cartesian combiner exploiting baseband summing can avoid the bandwidth limitations related to the other type of RF phase shifters, like vector modulators. This is to our knowledge the broadest relative bandwidth reported for a phased array front-end with antenna combining network at mmW.

TABLE I: Comparison Table with other Wideband structure

	This work	[2]#	[3]#	[6]∗	[5]∗
Frequency (GHz)	38.5-60.5 ¤	52-75	54-90	20-43	15.5-39
BW (GHz)	19.5 ¤	23	35.6	23	23.5
Gain (dB)	14.5-18 ¤	14	17	14.5	17
NF (dB)	6.2-8.1	4.8	5.4-7.4	5.5-8.2	3.6-9
Gain Control(bits)	4.5	NA	NA	cont.	cont.
IP1dB (dBm)	-33 to -26	NA	-15.7	-17	-11
Phase Var. (°)	0.6-5.4	NA	NA	0.2-5.4	1-6
LNA power(mW)	35#	32	19	NA	NA
VGA Power(mW)*	4 / VGA	NA	NA	30.3	104
Power per El.(mW)	63¤	NA	NA	NA	NA
Core area (mm^2)	0.175# 0.785¤	0.22	0.37	0.34	NA
Technology	28nm	90nm	65nm	65nm	SiGe

¤ Include LNAs, VGAs and combiner, # wideband LNA only ∗ VGA only

Acknowledgment

This research has been financially supported by Academy of Finland Ex5GRx (grant 2430226211) and also in part 6Genesis Flagship (grant 318927).

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