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Multilayer MoTe$_2$ Field-Effect Transistor at High Temperatures

Faisal Ahmed,* Abde Mayeen Shafi, David M. A. Mackenzie, Maaz Ahmed Qureshi, Henry A. Fernandez, Hoon Hahn Yoon, Md Gius Uddin, Markku Kuittinen, Zhipei Sun, and Harri Lipsanen*

Functional 2D material-based devices are likely subjected to high ambient temperatures when integrated into miniaturized circuits for practical applications, which may induce irreversible structural changes in materials and impact the device performance. However, majority of 2D devices’ studies focus on room temperature or low-temperature operation conditions. Here, the high-temperature (up to 673 K) electro-thermal response of molybdenum ditelluride (MoTe$_2$)-based field-effect transistors is investigated. The optimal annealing temperature of around 500–525 K for the multilayer MoTe$_2$ devices with two-fold enhancement in maximum current level, field-effect mobility, and current on-off ratio is identified. Furthermore, MoTe$_2$ devices show the transition of electrical response from gate modulation to the degenerately p-doped (hole dominant) characteristics when the operation temperature increases to $\approx$600 K. The gate-dependent electro-thermal measurements complemented by surface chemistry analysis confirm the near range hopping transport in the MoTe$_2$ channel at high temperature induced by thermally triggered oxidation of MoTe$_2$. These results not only provide the thermal endurance limits of MoTe$_2$ for practical applications, but also indicate the possible applications of MoTe$_2$ for thermal sensing applications.

1. Introduction

The carrier transport in a solid-state device is typically investigated at cryogenic temperatures to suppress the ambient effects. These studies are extremely useful to understand the pristine material characteristics and inherent device physics.[1,2] However, the functional devices are normally operated under high ambient temperatures, which are collectively induced by Joule heating, immediate environmental conditions, and large power dissipation density in compact integrated circuits.[3] As a result, the functional devices adversely suffer from unavoidable thermal stress. Similarly, most of the semiconducting 2D materials-based devices are likely vulnerable to large working temperatures than their bulk counterparts because of the large surface to volume ratio and poor thermal characteristics, i.e., low thermal conductivity and heat capacity.[4] It is, therefore, important to characterize the emerging semiconducting 2D materials such as MoTe$_2$ to high ambient temperatures for designing durable devices under practical operating conditions.

MoTe$_2$ is garnering increasing attention because of its rich polymorphic nature featuring semiconducting hexagonal (2H) phase, metallic distorted octahedral (1T’) phase, and superconducting crystalline phase.[5–7] The phase change energy barrier between 2H and 1T’ phases in MoTe$_2$ is significantly smaller ($<40$ meV) compared to other group VI-B based transition metal dichalcogenides (TMDCs).[5,8] Therefore, MoTe$_2$ is reported to be readily converted from 2H to 1T’ phase by laser irradiation,[5] electrostatic gate-induced doping,[9] Joule heating,[10] mechanical strain,[11] and irreversible growth by substitution doping.[12] Likewise, the material dissociation temperature for MoTe$_2$ is the lowest ($\approx$1000 K) compared to other counterpart TMDCs such as MoS$_2$ ($\approx$1150 K), and MoSe$_2$ ($\approx$1200 K),[13,14] because of small electronegativity difference (0.3) between molybdenum (Mo) and tellurium (Te) atoms.[15] Therefore, MoTe$_2$ is readily susceptible to thermally induced structural disorders compared to the other semiconducting TMDCs. For example, Te atoms in MoTe$_2$ are reported to dissociate at 473–523 K temperature.[14,16] These chemically and electrically active defects host ambient species and function as charge carrier trap sites, and mask the device...
response.\[17\] Therefore, the thermally sensitive nature of MoTe₂ demands careful attention under temperature treatments.

MoTe₂ devices are reported to induce polarity transition from n-type to p-type by thermal annealing to a specific temperature of 673 K.\[18\] Very recently, Liu et al. also reported polarity modulation in MoTe₂ devices at 423 K annealing temperature but with the opposite trend, i.e., from p-type to n-type.\[19\] In both the reported studies, the authors attributed the polarity transition to the thermally induced metal-MoTe₂ contact modifications, although the carrier transport in defective devices is governed by channel transport.\[20–22\] This motivates us to systematically investigate the carrier transport in MoTe₂ devices over a wide temperature window with a special focus on channel transport.\[17\]

Here, we designed controllable electro-thermal experiments from room temperature (RT) to high temperatures and employed to the back gate multilayer MoTe₂ field-effect transistors (FETs). First, we annealed the MoTe₂ devices to higher temperatures and collected device response at RT. The MoTe₂ devices showed more than two-fold enhancement in field effect mobility and current on-off ratio with a peak around 500–525 K temperatures due to decrease in contact resistance with temperature. Moreover, MoTe₂ devices surprisingly showed vanishing gate control to the degenerately p-doped characteristics at an increasing temperature from 300 to 600 K, which is caused by near range hopping transport in the defective MoTe₂ channel. The evolving p-type characteristics with enhanced conductance and mobility are caused by the thermally triggered oxidation of MoTe₂. We also exclude any speculation of temperature-induced phase change (up to 660 K temperature) from semiconducting 2H to the metallic 1T’ phase in MoTe₂ devices,\[19\] and this is further explained in a later part of the manuscript. Moreover, all measured MoTe₂ devices exhibit a non-negligible hysteresis window, which is defined as the threshold voltage difference during forward and backward V_G sweep, indicating the presence of unavoidable charge traps on MoTe₂. These charge traps could be attributed to surface adsorbrates, mobile ions in SiO₂, oxide traps close to the MoTe₂/SiO₂ interface, or intrinsic traps between layers as similarly described for MoS₂ devices on SiO₂.\[24\] Further details about hysteresis are given in Section S3 (Supporting Information).

After RT measurements, we systematically investigated the influence of the high temperature on the MoTe₂ FET performance in a nitrogen environment. At first, we employed a multistep annealing process with a sequential increase in the annealing temperature and returned to RT after each annealing cycle to collect device response data. We gradually annealed the device from 298 to 673 K by raising the temperature with a step of 25 K. Each annealing cycle was performed for 30 min. The annealing process is summarized in the step function plot in Figure 2a. The collected transfer curves at RT after each annealing cycle are shown in Figure 2b as a function of annealing temperatures. The obtained results showed a peak in I_D at 498 K. To further understand these results, we extracted field effect mobility (μ_FE) by linearly fitting the I_D–V_G plots after each annealing temperature using expression μ_FE = (dI_D/dV_G)(L/VOX V_D), where L and W are channel length and width and COX is gate oxide capacitance per unit area, which is 1.21 × 10⁻⁸ F cm⁻² for SiO₂ of 285 nm thickness. The average μ_FE and current on-off ratio at RT are plotted in Figure 2c after each annealing temperature. The average μ_FE and current on-off ratio values span in the range of 0.15–0.55 cm² V⁻¹ s⁻¹ and 80–200 respectively when plotted against annealing temperatures, with a marginal improvement at 498 K. We understand

2. Results and Discussion

Figure 1a,b show the schematic and optical image of a representative multilayer MoTe₂ back gate FET respectively. The RT transfer characteristics of the MoTe₂ device at a fixed source-drain voltage (V_D) of 1 V are collected by sweeping gate voltage (V_G) to ±100 V, as shown in Figure 1c. The Ni-contacted multilayer MoTe₂ device showed p-type (hole dominant) polarity probably due to high work function of Ni (5.04) and natural oxidation of MoTe₂ crystal. We emphasize the use of Ni for our experiment, because Ni will induce the smaller Schottky barrier for hole carriers by aligning Fermi-level close to the valence band edge of MoTe₂ as depicted in the inset of Figure 1c. Therefore, Ni will be helpful to realize channel dominant transport in MoTe₂ devices,\[23\] and this is further explained in a later part of the manuscript. Moreover, all measured MoTe₂ devices exhibit a non-negligible hysteresis window, which is defined as the threshold voltage difference during forward and backward V_G sweep, indicating the presence of unavoidable charge traps on MoTe₂. These charge traps could be attributed to surface adsorbates, mobile ions in SiO₂, oxide traps close to the MoTe₂/SiO₂ interface, or intrinsic traps between layers as similarly described for MoS₂ devices on SiO₂.\[24\] Further details about hysteresis are given in Section S3 (Supporting Information).

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that the obtained $\mu_{FE}$ values for MoTe$_2$ devices are low yet reasonable as reported elsewhere.$^{[25,26]}$ To get confident results, we repeated similar experiments to eight different thickness MoTe$_2$ devices from 15 to 65 nm and realized a similar peak in the range of 473–523 K annealing temperatures.

To understand these trends, we can categorize Figure 2b,c into three different regions based on annealing temperatures. The region I can be referred as the state when the device current, $\mu_{FE}$, and on-off ratio do not change with the temperature, i.e., 298 K to 398 K (purple color area in Figure 2c). In this region, the annealing temperatures are not high enough to induce any significant changes to device response. Region II, wherein the device performance was gradually increasing from 398 to 498 K (green color area in Figure 2c). Figure 2d shows the significant decrease in hysteresis window in region II, which indicates the removal of contaminations such as ambient absorbates, fabrication processing induced residues from scotch tape, and lithography polymers in MoTe$_2$ device.$^{[27]}$ Likewise, the annealing temperature might have improved the metal/MoTe$_2$ interface.$^{[18]}$ Therefore, we extracted contact resistance ($R_c$) along the metal/MoTe$_2$ interface after different annealing temperatures by employing four-probe method,$^{[28]}$ see Section S4 (Supporting Information). The obtained $R_c$ values from one of our measured MoTe$_2$ devices are given in Figure 2e. Similar to hysteresis, we did not observe any appreciable change in $R_c$ values at low annealing temperatures in region I, however, a significant reduction in $R_c$ is realized after annealing to 523 K, confirming contact improvement after annealing in region II. This also explains the improvement of device performance till optimal annealing temperatures. In region-III, the performance of the device decreases when the temperature increased to 673 K (light red color area in Figure 2c). We speculate the possibility

![Figure 2. Annealing results: a) The trend of gradual temperature increase during annealing measurements. Note that the device was annealed at a certain temperature for 30 min and each temperature step is 25 K. b) The obtained transfer plots at $V_D = 1$ V at RT after annealing to 673 K temperatures. c) The average field effect mobility and on-off ratio of the device at RT after each annealing temperature. The light blue, green, and brown colors represent regions I, II, and III of annealing temperature, respectively. Regions I and II: contact resistance dominated region. Region III: defect dominated region. d) The obtained Hysteresis window in $I_D-V_G$ plots after each annealing cycle. e) Contact resistance against $V_G$ after given annealing temperature values.](image-url)
of high temperature annealing induced structural changes in MoTe$_2$ in this region. It is reported that, the tellurium (Te) atoms in MoTe$_2$ start to decompose from 473 to 523 K, and this process becomes rigorous with further increasing temperature due to lowered formation energy.[34] Interestingly, the decomposition temperature coincides with the peak temperature in Figure 2b,c. Therefore, the high-temperature annealing in region III likely induces defects in MoTe$_2$, which is the possible cause of decrease in device performance. This is also confirmed by the hysteresis increase in region III initially. These trends also indicate that our MoTe$_2$ devices probably experienced crossover from contact-dominant to the channel-dominant transport after high-temperature annealing in region III due to formation of thermally induced defects in MoTe$_2$ channel.

In a nutshell, for improving adhesion with metal contacts and to formation of thermally induced defects in MoTe$_2$ channel. A recent study[35] also indicate that our MoTe$_2$ devices probably experienced crossover from contact-dominant to the channel-dominant transport after high-temperature annealing in region III due to formation of thermally induced defects in MoTe$_2$ channel.

Next, we simultaneously performed electrical measurements while increasing the stage temperature to 673 K in 25 K steps, as illustrated in Figure 3a. The temperature was stabilized for 3 min before performing measurements. Figure 3b shows the obtained transfer plots at similar $V_D$ and $V_G$ conditions with increasing temperature from 298 K (blue) to 673 K (red). We observed three main changes in device response with the temperature: i) with the increase in temperature, both on-state current and off-state current levels of the device monotonically increase; however, the increase in the off-state current is more pronounced than the on-state current. Thereby the current on-off ratio decreases with temperature, as shown in Figure 3c (red circles). ii) Within the same applied bias conditions, the gating effect of the device is diminished with temperature, and the MoTe$_2$ channel behaves like a degenerately p-doped at the higher temperature values. Alternatively, the minimum current level (off-state current) of the device is pushed toward more positive $V_G$, indicating that the chemical potential of the MoTe$_2$ channel is further shifted toward the valence band. iii) The $\mu_{FE}$ increases from 0.5 to 3 cm$^2$ V$^{-1}$ s$^{-1}$ up to 598 K, and then decreases rapidly to 673 K perhaps possibly due to material degradation induced by the repeatedly applied electrical and thermal stress. The observed increase of $\mu_{FE}$ with temperature is unlike previously reported trends for the other semiconducting TMDCs such as MoS$_2$, which shows a decrease in mobility with temperature (200–400 K) caused by strong electron–phonon interaction at elevated temperatures.[28] It is pertinent to note that the relatively thinner flakes <15 nm with Ti-contacts initially exhibited ambipolar characteristics (both electron and hole branches) due to different band offset formed with different contact metals.[30] Surprisingly, the thinner devices showed the transition from ambipolar to p-type conduction at high temperatures, nonetheless followed a similar temperature dependent electrical response, see Section S5 (Supporting Information). Previously, Chen et al. reported the multilayer MoTe$_2$ device showed the transition of MoTe$_2$ devices from n-type to the p-type transport after rapid thermal annealing to a single temperature of 673 K for mere 3 min.[18] Therefore, our high temperature results are consistent with their observed trend as our stabilization time at high temperature is 3–5 min. Additionally, we rule out any artifacts from metallic electrodes and SiO$_2$ at high temperature, since the applied highest temperature is well below their melting temperatures. Likewise, the gate leakage current remains stable even up to 673 K temperature. The flattening transfer curves, unusual $\mu_{FE}$–temperature trend, and rapidly decreasing on/off ratio with temperature, collectively indicate the temperature triggered drastic material change or an alternative carrier transport mechanism at elevated temperature.

Readers might speculate about the possible phase change from 2H to IT’ of MoTe$_2$ at high temperature,[31] as the applied maximum thermal energy (58 meV at 673 K) is higher than the formation energy for phase change. Above all, the IT’ phase is a semi-metal, which might be a possible cause of enhanced current level, and the low on-off ratio at high temperature, as explained in the previous paragraph. To address this speculation, we performed temperature-dependent Raman measurements to multilayer MoTe$_2$ flakes thanks to the noninvasive
nature of Raman spectroscopy. The as-exfoliated multilayer 2H-MoTe$_2$ exhibited two prominent Raman peaks at 173 and 233 cm$^{-1}$, attributed to the A$_{1g}$ and E$_{2g}$ vibration modes of MoTe$_2$[8] as shown in Figure 4. Subsequently, we collected the Raman spectra with increasing stage temperature from 83 to 663 K with 20 K temperature interval. For a better visibility, we only plot Raman spectra of MoTe$_2$ from 174 to 170 cm$^{-1}$, and 227 cm$^{-1}$ with temperature rise. The softening of Raman peaks with rising temperature is attributed to the thermal expansion of MoTe$_2$ lattice and anharmonic phonon coupling with higher temperature.[32] More importantly, the 1T' phase of MoTe$_2$ exhibits Raman-active modes around 125 cm$^{-1}$ and 140 cm$^{-1}$.[5,8] From Figure 4, we did not observe any sign of 1T' peaks even by increasing sample temperature to 663 K. These results suggest that multilayer MoTe$_2$ can withstand 663 K temperature without undergoing a phase change. These results further indicate the presence of alternative temperature dependent mechanisms responsible for modulating electrical characteristics in MoTe$_2$ at high temperature.

We recall that the $\mu_{\text{Eg}}$ in our MoTe$_2$ devices is very low ($\approx$1 cm$^2$ V$^{-1}$ s$^{-1}$) despite annealing to higher temperatures. These obtained $\mu_{\text{Eg}}$ values are significantly smaller than the theoretically predicted acoustic phonon-limited mobility of $\approx$2500 cm$^2$ V$^{-1}$ s$^{-1}$ for MoTe$_2$[13]. This large difference points toward the presence of a large number of native and/or thermally induced defects in our MoTe$_2$ devices.[36] As mentioned earlier, the most widely reported thermally induced defect-type in MoTe$_2$ is Te vacancies.[14,16] The Te vacancies either host neighboring Mo atoms to form Mo-Te antisites or more preferably ambient oxygen molecules due to their smaller size and abundance. Oxygen will physically and chemically adsorb and dissociate on MoTe$_2$ flake to form Mo-O and Te-O bonds at elevated temperatures. Interestingly, these are acceptor-type defects,[16] and induce trap states along the valence band edge, which might be a possible reason for the hole dominant transport in our MoTe$_2$ devices.[34] Although, all our measurements are performed in a nitrogen environment, we cannot rule out ambient oxygen adsorption on the MoTe$_2$ surface. To investigate the evolution of the surface chemical composition of MoTe$_2$, we performed X-ray photoemission spectroscopy (XPS) analysis before and after thermal treatments.

Figure 5a,b show the core-level XPS spectra of Mo3d and Te3d, respectively, for exfoliated, 473 K (region-II in Figure 2c) and 673 K (region-III in Figure 2c) treated MoTe$_2$ flakes. As shown in the lower panel of Figure 5a, the pristine MoTe$_2$ flakes exhibit a Mo 3d doublet around 231.6 eV (Mo3d$_{3/2}$) and 228.4 eV (Mo3d$_{5/2}$) corresponding to MoTe$_2$.[15,16] After annealing to 473 K (673 K), two additional peaks emerge at 234.6 eV (235.5 eV) and 231.5 eV (232.3 eV). These emerging peaks can be assigned to the Mo3d$_{3/2}$ and Mo3d$_{5/2}$ modes of MoO$_x$, respectively.[15,16] Similarly, the Te3d doublet for pristine MoTe$_2$ flakes are located at 583.3 eV (Te3d$_{3/2}$) and 573 eV (Te3d$_{5/2}$), as can be seen in lower panel in Figure 5b. After 473 K (673 K) temperature treatments, a new doublet emerges at 586.4 eV (587 eV) and 576 eV (576.7 eV). The new locations are typically for TeO$_2$.[15,16] These emerging peaks along with smearing out of MoTe$_2$ peaks confirm that the top surface of MoTe$_2$ is mostly converted to MoO$_x$ and TeO$_2$ at higher temperatures. In addition to this, MoO$_x$ peaks at 673 K temperature depict extra shoulders, which can be attributed to the presence of different oxidation states of Mo such as MoO$_3$, MoO$_2$ and MoO on MoTe$_2$ surface. Furthermore, the binding energy is associated with the chemical potential in the materials, and therefore the shift in binding energy provides useful information about the nature of doping in a material.[17,26]
We realized negative shifts in Mo\(^{4+}\) and Te\(^{2-}\) peaks with temperature, i.e., Mo3d peaks redshift around 0.1 eV at 473 K and 0.4 eV at 673 K, and Te3d modes redshift by 0.01 eV at 473 K and 0.04 eV at 673 K, with respect to those of the pristine flake. The gradual decrease in binding energies with temperature depicts the progressive chemical potential reduction in MoTe\(_2\) and thereby controllable p-doping with temperature in MoTe\(_2\). In brief, the annealing up to 473 K induces mild oxidation of the top surface which leads to improvement of device performance in MoTe\(_2\) with slight p-doping effect. However, the strong oxidation of MoTe\(_2\) flakes is realized with formation of Mo- and Te-based amorphous oxides on their surface at elevated temperature with strong p-doping effect. In addition to this, we also performed atomic force microscopy analysis on freshly exfoliated MoTe\(_2\) flakes before and after thermal treatment, see Section S7 (Supporting Information). Interestingly, the results showed a slight increase in flake thickness from \(\approx 0.27\) nm and RMS roughness increases from \(\approx 0.113\) to 0.329 nm. The increase in thickness and roughness after thermal treatment probably indicates the formation of amorphous oxides, i.e., MoO\(_x\) and TeO\(_2\) on the MoTe\(_2\) surface after thermal treatment, which are reported to be relatively thicker, i.e., \(\approx 2\) nm thick.\(^{26,36}\) These observations further support the thermo-oxidation of MoTe\(_2\) surface.

In a defective device with a channel-dominated transport, the charge carriers are localized around the defect sites, and their transport is governed by a hopping mechanism.\(^{20,22,37}\) The channel-dominated transport in our MoTe\(_2\) devices can be confirmed by measuring the Schottky barrier height (SBH) along the metal/MoTe\(_2\) interface by employing the thermionic emission model,\(^{38}\) see Section S8 (Supporting Information) for more details. Note that the SBH extraction in channel-dominant devices might lead to considerable error. Therefore, we only use the data set shown in Figure 3b at relatively lower temperatures, i.e., 298 to 373 K to minimize the impact of high temperature induced channel defects. The obtained effective SBH values in Figure 6a decrease from 0.15 eV at \(V_G = 0\) to 0.075 eV at \(V_G = -100\) V because of the p-type nature of our MoTe\(_2\) device. More importantly, the small SBH values further manifest the presence of channel dominant transport in our MoTe\(_2\) devices. The hopping transport can be confirmed by fitting temperature dependent electrical results as \(G \propto \exp \left[-\left(T_o/T\right)^\gamma\right]\), where \(G\) is conductance, \(T\) is temperature, \(T_o\) is the ambient temperature, and \(\gamma\) is constant whose value varies from 0.25 to 1 depending on the dimensionality of the system.\(^{20}\) At high temperature, the \(G\) readily changes by temperature with \(\gamma = 1\), representing the thermally activated near neighbor hopping (NNH) transport. Therefore, we plotted the temperature dependent \(G\) near off-state at \(V_G = 100\) V from 373 to 625 K temperature in Figure 6b. The linear fit of logarithmic of \(G\) as a function of \(T^{-1}\) provides an excellent depiction of the disordered MoTe\(_2\) conduction channel. A small deviation of fits after 0.00118 K\(^{-1}\) is due to the degradation of the MoTe\(_2\) channel at higher temperatures as mentioned earlier. We further extract activation energy (\(E_a\)) from thermally activated NNH model as \(G \propto \exp \left[-\left(E_a/k_BT\right)^\gamma\right]\), where \(k_B\) is the Boltzmann constant.\(^{20–22}\) Figure 6c shows the \(E_a\) as a function of \(V_G\) by fitting the Arrhenius plot between logarithmic of \(G\) and \(T^{-1}\). The obtained \(E_a\) values vary from 0.22 to 0.12 eV when \(V_G\) was swept from 0 to 100 V, which approximately depicts the energy depth of charge traps around the valence band maxima. Additionally, the modulation of \(E_a\) with respect to \(V_G\) also suggests presence of more than one types of oxygen traps, as explained in previous paragraph. Our MoTe\(_2\) samples are exhibiting more p-type behavior at high temperature, therefore, there is more probability of oxidation defects instead of Te vacancies because the chalcogenide vacancies in semiconducting TMDCs are typically reported to induce defect states close to the conduction band edge.\(^{34}\) Liu et al. reported charge traps depth of around 0.24 to 0.018 eV depending on applied \(V_G\),\(^{19}\) and interestingly our measured \(E_a\) range agrees with their provided numbers. With the increase of temperature, more charge carriers gain sufficient energy to surmount the defect states energy barrier. Therefore, we realize

Figure 6. Hopping transport in MoTe\(_2\) device with defective channel: a) Effective Schottky barrier height at Ni/MoTe\(_2\) interface plotted against the applied \(V_G\). b) Plot of minimum channel conductance at \(V_G = 100\) V as a function of inverse temperature. The red line denotes the thermally activated NNH mechanism. c) The extracted activation energy plotted against applied \(V_G\). Note that all data in Figure 6a–c are taken from the same device measured in Figure 3. (d) and (e) are the illustration of transport in defective MoTe\(_2\) channel at low- and high-temperature conditions, respectively, where dashed line represents the position of Fermi level in the channel.
the monotonic increase in current density, conductance, and mobility with temperature caused by hopping of charge carriers via oxidation traps. However, with the decrease in temperature, the charge carriers are frozen in defect states as they cannot get enough thermal energy to jump out of the trap site. As a result, the electrical response of the device is almost restored at lower temperature values. This explains the observed discrepancy in Figures 2b and 3b. During annealing measurements, we measured our MoTe2 devices at RT, therefore, the charge traps did not contribute to the device response, as shown in Figure 6d. However, during high temperature experiments, we measured electrical response at elevated temperature, see Figure 6e, and therefore we realize enhancement in device response.

Our results point toward several important perspectives for MoTe2 usage for future applications. The p-doping effect observed here in MoTe2 is realized without any introduction of intentional dopant. This natural ambient oxygen doping effect triggered by high temperature can be utilized to selectively control the electrical response of MoTe2 to realize complementary devices for electronic and optoelectronic applications.[31, 32] However, the controllability and homogeneity of this doping process can be characterized by employing spatial characterization equipment, such as scanning tunneling microscopy and/or Kelvin probe microscopy in controlled environments.[33, 34] In addition to this, for electronics applications perspective, wherein stable device operation is required, it is recommended to passivate MoTe2 flakes with capping materials such as hexagonal boron nitride to avoid ambient oxygen exposure.[35] Lastly, these results can be guidelines to use MoTe2 devices for potential thermal sensing and memory applications. In fact, recently, localized heating was used to investigate MoTe2-based resistive memory device.[36]

In conclusion, we systematically investigated the electrical response of multilayer MoTe2 devices under large ambient temperatures in a controllable fashion. We identified the optimal post-fabrication annealing temperature for MoTe2. Furthermore, MoTe2 devices showed thermal endurance over 598 K even with repeated electrical and thermal stress. Lastly, the charge transport at high temperature in MoTe2 device is governed by thermally triggered ambient oxidation. Our results will help provide useful information to design practical and durable devices and open up new avenues for future device applications.

3. Experimental Section

Sample Preparation: The multilayer MoTe2 flakes were mechanically exfoliated from the commercially available bulk MoTe2 source (2D Semiconductors) via a typical scotch-tape technique on a p-doped silicon substrate (0.001–0.005 Ω cm) covered with a 285 nm thick thermally grown SiO2. After exfoliation, electron beam lithography (EBL Vistec, EBPG 5000) and metallization was carried out by using electron beam evaporator (MASA, IM-9912) under ~10−7 torr chamber pressure to deposit 5 nm Ni or Ti adhesion layer followed by 50 nm thick Au to form the electrodes. The height and roughness of the targeted flakes were determined using an atomic force microscope (Bruker, Dimension Icon), see Sections S2 and S7 (Supporting Information).

Electrical and High-Temperature Measurements: All the electrical measurements were carried out with a custom-built setup based on a Linkam LN600-P probe station with environmental and temperature controller (T96-S) using a source-measure unit (Keithley 2400) and a Keithley 2700 multiplexing/voltage measurement unit, as described here.[37] The measurement system was capable of achieving 150 °C min−1 heating rate and 100 °C min−1 cooling rate with <0.1 °C temperature stability. All the measurements were repeated twice at each point to get confident data.

Raman Spectroscopy: Raman signals were collected by employing confocal micro-Raman (WITec alpha300 RA+) in the conventional mode with 532 nm excitation laser at 1 mW power. The sample was placed in a cryostat cooled Linkam chamber via liquid nitrogen, and the chamber temperature was varied from 83 to 663 K temperature.

X-Ray Photoelectron Spectroscopy: The XPS measurements were performed with Kratos Axis Ultra, equipped with a monochromatic Al Kα (1486.96 eV) source. The wide scans were performed with 300 × 700 μm analysis area. The high-resolution scans were performed with 20 eV pass energy and with 0.1 eV energy step. All spectra were calibrated by the C1s peak at 284.6 eV.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

annealing, electro-thermal response of MoTe2 at high temperatures, field-effect transistors, hopping transport, molybdenum ditelluride, oxidation of MoTe2