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Multifunctional Cascade Control of Voltage-Source Converters Equipped With an *LC* Filter

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***Abstract*—This article proposes a multifunctional cascade controller structure for voltage-source converters. The proposed structure contains a decoupling loop between the outer voltage control loop and the inner current control loop, and operation in either voltage or current control mode is possible. In voltage control mode, the current controller can be made completely transparent. In the case of faults, the proposed structure enables inherent overcurrent protection by a seamless transition from voltage to current control mode, wherein the current controller is fully operational. Seamless transitions between the control modes can also be triggered with an external signal to adapt the converter to different operating conditions. The proposed structure allows for integration of simple, accurate, and flexible overcurrent protection to state-of-the-art single-loop voltage controllers without affecting voltage control properties under normal operation. The properties of the proposed controller structure are validated experimentally on a 10-kVA converter system.**

***Index Terms*—AC-voltage control, cascade control, current control, overcurrent protection, voltage-source converters (VSCs).**

I. Introduction

THE paradigm shift toward clean energy production has sparked a significant interest in microgrids and stand-alone converters powered by distributed renewable energy generation. Consequently, the use of voltage-source converters (VSCs) operating as ac-voltage sources is on the rise. In addition to grid applications [1]–[4], such VSCs find use in, e.g., uninterruptible power supplies [5], dynamic voltage restorers [6], and a variety of other stand-alone systems [7]–[9]. In all of the aforementioned applications, the VSC system is typically equipped with an *LC* filter.

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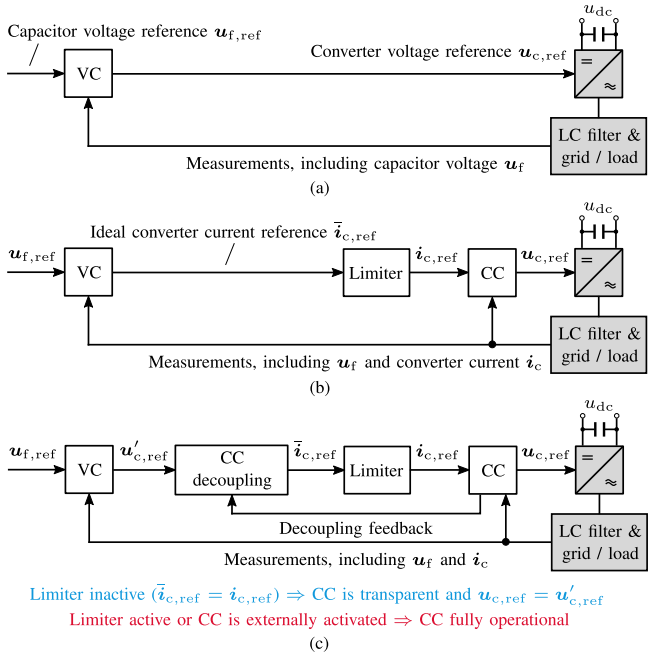

Fig. 1. Simplified block diagram of (a) single-loop voltage controller (b) conventional cascade controller (c) proposed cascade controller, where the inner controller dynamics can be made either partially or completely transparent in voltage control mode when the current reference limiter is not active. VC stands for voltage controller and CC stands for current controller.

A significant research effort has been devoted to developing ac-voltage control, henceforth referred to as voltage control, algorithms for VSCs. As a result, several different control methods have been proposed with distinct properties. Considering linear controllers, the majority of the voltage control algorithms can be roughly divided into single-loop [9]–[14] and cascade [3]–[5], [8], [15], [16] control algorithms. Nonlinear methods based on, e.g., model-predictive [17], [18] and sliding-mode [19], [20] control, have also been proposed. Whereas the single-loop controllers [cf. Fig. 1(a)] can be considered as a single entity that generates the actuator reference based on the input reference and a set of measurements, the cascaded controllers [cf. Fig. 1(b)] have a clear hierarchical structure with the outer-loop controllers providing their successor a reference signal. In this article, the cascade controller consists of an outer voltage control loop that controls the filter capacitor voltage and an inner current control

loop that controls the converter current. It should be noted that the division between single-loop and cascade controllers is not explicit, as it has been shown that certain cascade controllers have an equivalent single-loop controller [21].

In general, there are certain tradeoffs in choosing between the single-loop and cascade structures. Single-loop controllers can typically achieve higher bandwidth as compared to cascade controllers with dynamics in the inner current controller. This is due to the dynamical coupling of the control loops in the aforementioned cascade controllers, which limits the achievable bandwidth of the outer control loop. In practice, the bandwidth of the outer control loop should be maintained several times lower than that of the inner control loop [6], [8]. On the other hand, given that the converter current is controlled in the inner control loop, the cascade structure allows for inherent overcurrent protection through limitation of the current reference [cf. Fig. 1(b)].

In addition to a good dynamic performance and robustness to variations in the filter parameters and loads, converter overcurrent protection is an important, yet typically overlooked, aspect of the voltage controller design. The semiconductor switches in the converter have very limited tolerance for currents exceeding their maximum value due to their low thermal inertia [22]. Therefore, a fast-acting current limitation mechanism is mandatory in practice. The current limitation can either be based on the hardware [23], the software, i.e., the controller [24]–[31], or their combination [32], [33]. These mechanisms can be designed to either trip the converter or to limit its current below a threshold value while remaining operational. In general, it is more favorable to have the option for the converter to remain operational during overcurrent situations, e.g., for fault-ride through in grid applications [29] or for critical loads in stand-alone applications [31].

Most of the state-of-the-art software-based overcurrent protection schemes are based on either altering the controller structure [23], [30]–[33] or using cascade controllers with dynamic states in the inner current loop, e.g., an integrator or a resonator [25]–[29]. Altering the controller structure during operation requires careful maintenance of the dynamic states in the control loops, as improperly set dynamic states can have an adverse effect on the transient response following a change in the controller structure [34]. Furthermore, overcurrent protection schemes relying on controller alteration tend to require some fault detection mechanism [23], [24], [32], [33], which further increases the complexity of the system.

In the recently proposed high-performance single-loop voltage controllers [11]–[14], the aspect of overcurrent protection is either neglected [11], requires additional fault detection mechanism and results in tripping of the converter [12], or relies on modification of the pulsewidth modulator (PWM) reference [13], [14]. The overcurrent protection capability of these methods does not rival that of properly designed cascade controllers.

It would be of great interest to obtain a current limitation mechanism for the single-loop voltage controllers, such as [11]–[14], with the simplicity, accuracy, and flexibility enabled by the cascade controller structure while retaining the original properties of these voltage controllers under normal operation. In an effort to meet this demand, this article presents a multifunctional cascade controller structure [cf. Fig. 1(c)] with the following properties.

1) Operation in either voltage or current control mode without any modifications to the controller structure is possible.
2) The proposed structure can be used flexibly to turn the inner controller either partially or completely transparent in voltage control mode while the inner-loop reference is not limited. Consequently, the properties, e.g., dynamic performance and robustness to load variations, of the two control modes can be set independently of each other. This allows for integration of simple and accurate overcurrent protection to single-loop voltage controllers without having an effect on their original properties under normal operating conditions.
3) The proposed structure enables seamless transitions between the control modes. The transitions can be triggered by either saturation of the inner-loop reference or with an external signal. The possibility of transitioning between control modes at will can be useful in grid applications, where the converter may have to operate in either grid-forming or grid-connected mode [2].

The properties of the proposed cascade controller structure are experimentally validated on a 10-kVA converter.

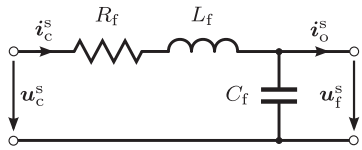

Fig. 2. Circuit model of an LC filter in stationary coordinates.

II. System Model

A three-phase converter equipped with an LC filter and without a neutral wire is considered. Fig. 2 shows the circuit diagram of an LC filter in stationary coordinates (indicated by the superscript s in the signals). The converter voltage is denoted by $\boldsymbol{u}_\mathrm{c}^\mathrm{s}$, the converter current by $\boldsymbol{i}_\mathrm{c}^\mathrm{s}$, the capacitor voltage by $\boldsymbol{u}_\mathrm{f}^\mathrm{s}$, and the load current by $\boldsymbol{i}_\mathrm{o}^\mathrm{s}$. The LC filter in stationary coordinates is defined by the state-space model

$$\frac{d}{dt}\underbrace{\begin{bmatrix}\boldsymbol{i}_\mathrm{c}^\mathrm{s}\\ \boldsymbol{u}_\mathrm{f}^\mathrm{s}\end{bmatrix}}_{\mathbf{x}^\mathrm{s}} = \underbrace{\begin{bmatrix}-\frac{R_\mathrm{f}}{L_\mathrm{f}} & -\frac{1}{L_\mathrm{f}}\\ \frac{1}{C_\mathrm{f}} & 0\end{bmatrix}}_{\mathbf{A}}\mathbf{x}^\mathrm{s} + \underbrace{\begin{bmatrix}\frac{1}{L_\mathrm{f}}\\ 0\end{bmatrix}}_{\mathbf{B}_\mathrm{c}}\boldsymbol{u}_\mathrm{c}^\mathrm{s} + \underbrace{\begin{bmatrix}0\\ -\frac{1}{C_\mathrm{f}}\end{bmatrix}}_{\mathbf{B}_\mathrm{o}}\boldsymbol{i}_\mathrm{o}^\mathrm{s} \quad (1)$$

where the filter inductance and capacitance are denoted by L_f and C_f, respectively. The resistance R_f models the losses in the filter inductor. The undamped angular resonance frequency of the filter is obtained as

$$\omega_\mathrm{r} = \frac{1}{\sqrt{C_\mathrm{f}L_\mathrm{f}}}. \quad (2)$$

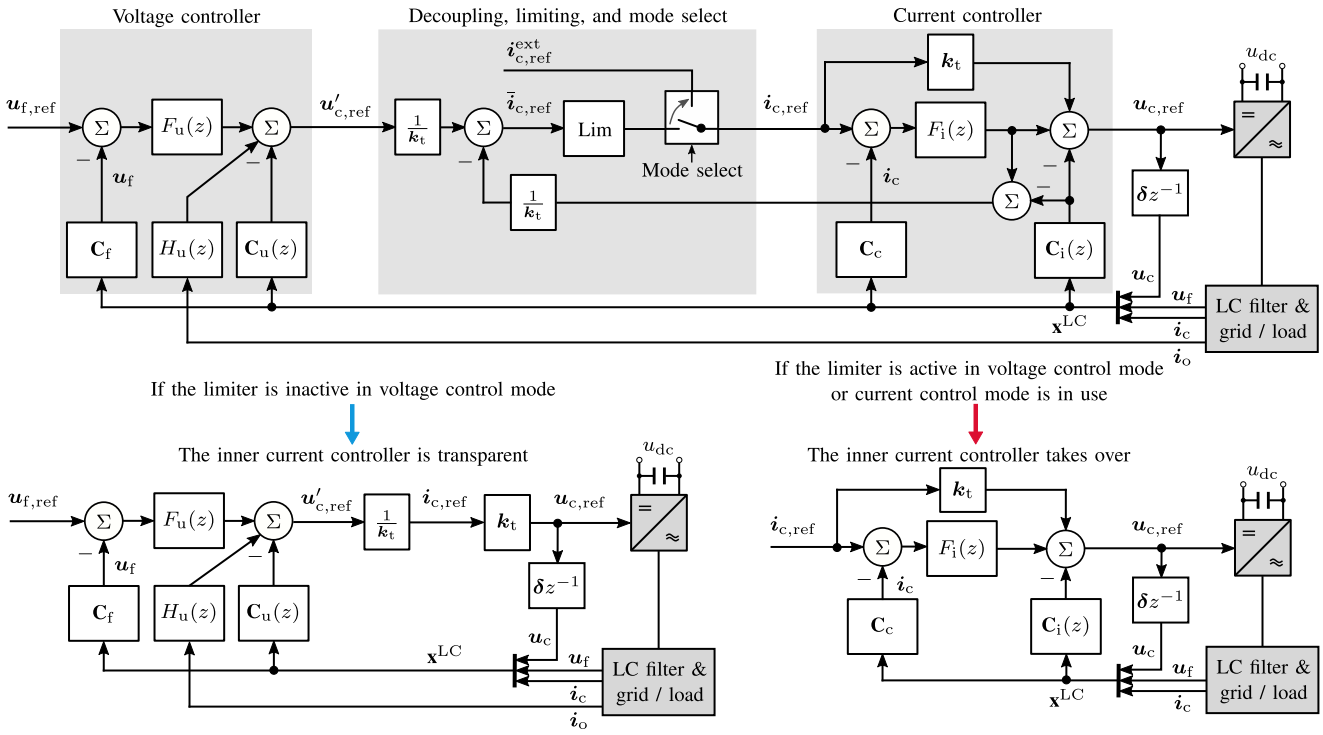

Fig. 3. Block diagram of the proposed cascade controller structure. The controller can be divided into the following three parts: the voltage controller; decoupling, limiting, and mode selection section; and the current controller. Depending on the control mode and whether the inner-loop reference saturation is active, the controller appears differently. The state vector $\mathbf{x}^{\mathrm{LC}}$ is defined as $\mathbf{x}^{\mathrm{LC}} = [\boldsymbol{i}_{\mathrm{c}}, \boldsymbol{u}_{\mathrm{f}}, \boldsymbol{u}_{\mathrm{c}}]^{\mathrm{T}}$, resulting in $\mathbf{C}_{\mathrm{f}} = [0, 1, 0]$ and $\mathbf{C}_{\mathrm{c}} = [1, 0, 0]$.

While the proposed structure is applicable to controllers in both stationary and synchronous coordinates, the system is analyzed in synchronous coordinates using complex space vectors, e.g., the capacitor voltage is $\boldsymbol{u}_{\mathrm{f}} = u_{\mathrm{fd}} + ju_{\mathrm{fq}}$.

III. Proposed Multifunctional Cascade Controller Structure

The main contribution of this article, the proposed multifunctional cascade controller structure, is presented in this section. A block diagram of the proposed structure is shown in Fig. 3. The controller structure can be divided into the following three parts: the voltage controller; the decoupling, limiting, and mode selection section; and the current controller. These parts are further discussed in the following subsections. The structure allows for making the inner current loop either partially or completely transparent in voltage control mode when the inner-loop reference is not limited. On the other hand, when the reference is limited, the current loop takes over, and seamless transition to current control mode occurs. Consequently, the proposed structure can be used to augment single-loop voltage controllers with overcurrent protection without affecting the controller properties during normal operation, i.e., when the inner-loop controller reference is not limited. An example of this augmentation is presented in Section IV.

A. Voltage Controller

The voltage controller in Fig. 3 is defined by the single-input single-output (SISO) transfer functions $F_{\mathrm{u}}(z)$ and $H_{\mathrm{u}}(z)$, the output vector $\mathbf{C}_{\mathrm{f}} = [0, 1, 0]$, and a multiple-input single-output (MISO) transfer function $\mathbf{C}_{\mathrm{u}}(z)$ with three inputs.[1] The inputs to $\mathbf{C}_{\mathrm{f}}$ and $\mathbf{C}_{\mathrm{u}}(z)$ are defined by the state vector $\mathbf{x}^{\mathrm{LC}} = [\boldsymbol{i}_{\mathrm{c}}, \boldsymbol{u}_{\mathrm{f}}, \boldsymbol{u}_{\mathrm{c}}]^{\mathrm{T}}$, cf. Appendix. The transfer function $F_{\mathrm{u}}(z)$ is used to eliminate the capacitor voltage error $\boldsymbol{u}_{\mathrm{f,ref}} - \boldsymbol{u}_{\mathrm{f}}$ and the transfer function $H_{\mathrm{u}}(z)$ from the load current $\boldsymbol{i}_{\mathrm{o}}$ can be used to include disturbance feedforward for the voltage controller, e.g., as in [14], [16], and [28], to improve disturbance rejection properties of the controller. The MISO transfer function $\mathbf{C}_{\mathrm{u}}(z)$ can be used to add active damping.

If the proposed cascade controller structure is used to augment a single-loop voltage controller with multifunctionality, the only prospective modifications imposed by the proposed structure on the single-loop voltage controller are related to the scaling of the antiwindup signals responsible for limiting the dynamic states of the controller during output saturation [35]–[37]. Moreover, proper maintenance of the dynamic states of the augmented voltage controller during externally forced current control mode allows seamless transition back to voltage control mode. Explicit guidelines related to these two aspects cannot be given, as they are specific to the structure of the augmented single-loop voltage controller. However, an example case with an integrator is given in Section IV.

[1] In case of a PI-type voltage controller with proportional gain $\boldsymbol{k}_{\mathrm{p}}$ and integral gain $\boldsymbol{k}_{\mathrm{i}}$ as, e.g., in [29], the transfer functions become $F_{\mathrm{u}}(z) = \boldsymbol{k}_{\mathrm{p}} + \boldsymbol{k}_{\mathrm{i}}/(z-1)$, $H_{\mathrm{u}}(z) = 0$, and $\mathbf{C}_{\mathrm{u}}(z) = [0, 0, 0]$.

B. Current Controller

The current controller in Fig. 3 is defined by a reference feedforward through gain $\boldsymbol{k}_\mathrm{t}$, a SISO transfer function $F_\mathrm{i}(z)$, the output vector $\mathbf{C}_\mathrm{c} = [1, 0, 0]$, and a MISO transfer function $\mathbf{C}_\mathrm{i}(z)$ with three inputs.[2] As for the corresponding transfer functions of the voltage controller, the inputs to $\mathbf{C}_\mathrm{c}$ and $\mathbf{C}_\mathrm{i}(z)$ are defined by the state vector $\mathbf{x}^\mathrm{LC} = [\boldsymbol{i}_\mathrm{c}, \boldsymbol{u}_\mathrm{f}, \boldsymbol{u}_\mathrm{c}]^\mathrm{T}$. The purpose of $\boldsymbol{k}_\mathrm{t}$ is to improve reference tracking dynamics and of $F_\mathrm{i}(z)$ to eliminate the converter current error $\boldsymbol{i}_\mathrm{c,ref} - \boldsymbol{i}_\mathrm{c}$. The MISO transfer function $\mathbf{C}_\mathrm{i}(z)$ can be used to add active damping and to improve disturbance rejection.

For the proposed structure to be applicable, the open-loop transfer function from $\boldsymbol{i}_\mathrm{c,ref}$ to $\boldsymbol{u}_\mathrm{c,ref}$ must have a direct feedthrough term. This is equivalent to stating that the transfer function must have a relative degree of zero, i.e., the transfer function should be proper, but not strictly proper. As a consequence, the open-loop transfer function from $\boldsymbol{i}_\mathrm{c,ref}$ to $\boldsymbol{u}_\mathrm{c,ref}$ can be written as

$$\frac{\boldsymbol{u}_\mathrm{c,ref}(z)}{\boldsymbol{i}_\mathrm{c,ref}(z)} = \boldsymbol{k}_\mathrm{t} + F_\mathrm{i}(z) \tag{3}$$

where the transfer function $F_\mathrm{i}(z)$ is strictly proper, i.e., the order of its denominator polynomial is greater than the order of its numerator polynomial. This is the sole requirement imposed by the proposed structure. As explained in what follows, the reference feedforward path through the gain $\boldsymbol{k}_\mathrm{t}$ allows simple decoupling of the current controller dynamics determined by $F_\mathrm{i}(z)$ and $\mathbf{C}_\mathrm{i}(z)$ while in voltage control mode and under linear operation, making the current controller transparent.

C. Decoupling, Limiting, and Mode Selection

The middle section in Fig. 3 together with the feedback from the dynamic states of the current controller is responsible for transforming the inner current controller completely transparent, determining the control mode, and protecting the converter from overcurrent.

1) Decoupling: In the figure, the inner current control dynamics are made completely transparent. This is realized by feeding back the inner-loop controller dynamics, determined by the transfer functions $F_\mathrm{i}(z)$ and $\mathbf{C}_\mathrm{i}(z)$, to the input of the inner-loop reference limiter through a decoupling gain $\boldsymbol{k}_\mathrm{t}^{-1}$. The output from the voltage controller $\boldsymbol{u}'_\mathrm{c,ref}$ is similarly scaled by the decoupling gain. Assuming that the limiter is inactive, i.e., $\bar{\boldsymbol{i}}_\mathrm{c,ref} = \boldsymbol{i}_\mathrm{c,ref}$, the equation for converter voltage reference can then be written as

$$\boldsymbol{u}_\mathrm{c,ref}(k) = [\boldsymbol{k}_\mathrm{t} + F_\mathrm{i}(z)]\boldsymbol{i}_\mathrm{c,ref}(k) - F_\mathrm{i}(z)\boldsymbol{i}_\mathrm{c}(k) - \mathbf{C}_\mathrm{i}(z)\mathbf{x}^\mathrm{LC}(k). \tag{4}$$

Writing the converter current reference in terms of the voltage controller output $\boldsymbol{u}'_\mathrm{c,ref}$ and the feedback from the dynamic states of the current controller, one obtains

$$\boldsymbol{i}_\mathrm{c,ref}(k) = \frac{\boldsymbol{u}'_\mathrm{c,ref}(k) + F_\mathrm{i}(z)\boldsymbol{i}_\mathrm{c}(k) + \mathbf{C}_\mathrm{i}(z)\mathbf{x}^\mathrm{LC}(k)}{\boldsymbol{k}_\mathrm{t} + F_\mathrm{i}(z)}. \tag{5}$$

Placing this into (4) yields

$$\boldsymbol{u}_\mathrm{c,ref}(k) = [\boldsymbol{k}_\mathrm{t} + F_\mathrm{i}(z)]\frac{\boldsymbol{u}'_\mathrm{c,ref}(k) + F_\mathrm{i}(z)\boldsymbol{i}_\mathrm{c}(k) + \mathbf{C}_\mathrm{i}(z)\mathbf{x}^\mathrm{LC}(k)}{\boldsymbol{k}_\mathrm{t} + F_\mathrm{i}(z)} - F_\mathrm{i}(z)\boldsymbol{i}_\mathrm{c}(k) - \mathbf{C}_\mathrm{i}(z)\mathbf{x}^\mathrm{LC}(k) = \boldsymbol{u}'_\mathrm{c,ref}(k). \tag{6}$$

The abovementioned equation shows that if the limiter is not active, the decoupling feedback cancels the effect of current controller dynamics from the converter voltage reference $\boldsymbol{u}_\mathrm{c,ref}$ through the static reference feedforward with gain $\boldsymbol{k}_\mathrm{t}$. On the other hand, if the current reference is limited, i.e., $\bar{\boldsymbol{i}}_\mathrm{c,ref} \neq \boldsymbol{i}_\mathrm{c,ref}$, the decoupling is not active and the current controller takes over.

Remark 1: The inner current controller can be made partially transparent by omitting specific modes from the feedback of the current controller dynamics, e.g., by using partial fraction decomposition.

2) Limiting: To enable overcurrent protection of the converter, the converter current reference is limited, depicted by a limiter function block in Fig. 3. Several different limiter functions with different properties, including latched and instantaneous limiting [26], [29], distortion-free limiting [38], and phase-specific root mean square (RMS) limiting [27], [32], have been proposed. The choice of the limiter function is based on the requirements imposed by the application.

3) Mode Selection: The cascade structure also allows for manual transition between voltage and current control modes by bypassing the outer voltage loop and directly feeding the desired current reference $\boldsymbol{i}^\mathrm{ext}_\mathrm{c,ref}$ to the inner current loop. This feature, which can be used, e.g., in grid-tied converters to transition between grid-forming and grid-connected modes [2], is depicted by a switch in Fig. 3.

IV. Application Example

To demonstrate the benefit of the proposed structure, a state-feedback voltage controller based on the controller recently proposed in [14] is augmented with overcurrent protection and possibility of operating in current control mode by using the proposed cascade structure. A state-feedback controller is employed in the inner loop as well. The converter phase currents and capacitor line-to-line voltages are measured for the cascade controller. In addition, the dc-link voltage u_dc is measured for the PWM. As state-feedback control has been thoroughly analyzed for power conversion applications, a brief presentation is settled on. For a more detailed treatment, the interested reader is referred to, e.g., [12], [14], [39]–[41], and the references cited therein.

A. Inner Current Loop

As per usual with cascade controllers, the controller design is commenced from the innermost loop. A block diagram of the example controller is shown in Fig. 4. The inner current controller design is based on the assumption of an L filter plant

[2] In case of a PI-type current controller with proportional gain $\boldsymbol{k}_\mathrm{p}$ and integral gain $\boldsymbol{k}_\mathrm{i}$ combined with direct capacitor voltage feedforward as, e.g., in [27], the transfer functions become $\boldsymbol{k}_\mathrm{t} = \boldsymbol{k}_\mathrm{p}$, $F_\mathrm{i}(z) = \boldsymbol{k}_\mathrm{i}/(z-1)$ and $\mathbf{C}_\mathrm{i}(z) = [\boldsymbol{k}_\mathrm{p}, -1, 0]$.

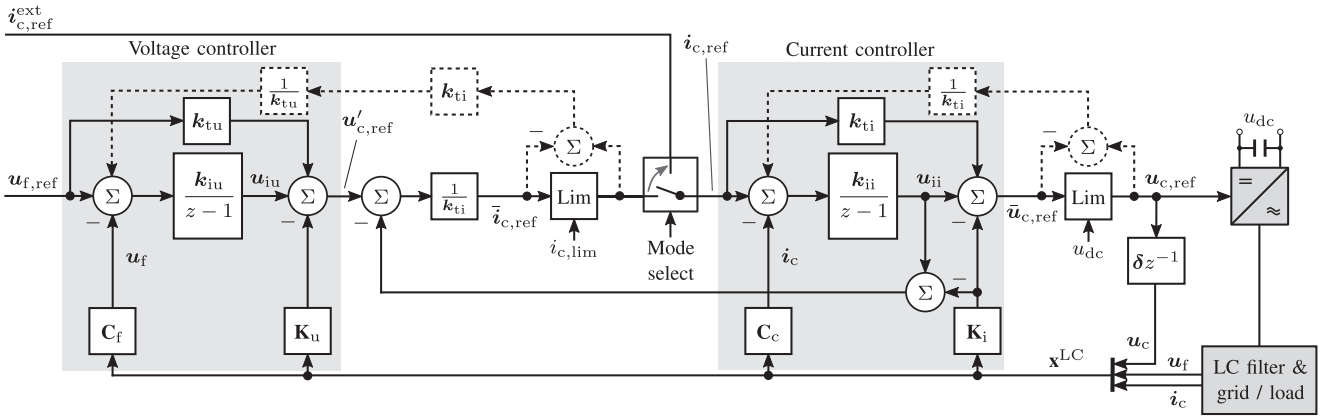

Fig. 4. Block diagram of the example controller implemented in the proposed cascade controller structure. A limiter block with input from the outer control loop is used to saturate the inner-loop reference for overcurrent protection. A realizable reference antiwindup mechanism, marked with dashed lines in both the inner and the outer loops, is used.

defined by (21) in the Appendix. The formulation of a state-feedback current controller for an L filter plant can be considered to be a simplification of the state-feedback current control of an LCL filter plant [39], [40] and analogous to the state-feedback current control of synchronous motor drives [41]. In accordance with Fig. 4, the control law for the inner current loop becomes

$$\bar{\boldsymbol{u}}_{\mathrm{c,ref}}(k) = \boldsymbol{k}_{\mathrm{ti}}\boldsymbol{i}_{\mathrm{c,ref}}(k) + \boldsymbol{u}_{\mathrm{ii}}(k) - \mathbf{K}_{\mathrm{i}}\mathbf{x}^{\mathrm{LC}}(k) \tag{7}$$

$$\boldsymbol{u}_{\mathrm{ii}}(k+1) = \boldsymbol{u}_{\mathrm{ii}}(k) + \boldsymbol{k}_{\mathrm{ii}}[\boldsymbol{i}_{\mathrm{c,ref}}(k) - \boldsymbol{i}_{\mathrm{c}}(k)] \tag{8}$$

where $\bar{\boldsymbol{u}}_{\mathrm{c,ref}}$ is the ideal converter voltage reference, $\boldsymbol{k}_{\mathrm{ti}}$ is the reference feedforward gain, $\boldsymbol{u}_{\mathrm{ii}}$ is the integral state, $\mathbf{K}_{\mathrm{i}}$ is the state-feedback gain vector, and $\boldsymbol{k}_{\mathrm{ii}}$ is the integral gain. The integral state is included to achieve zero steady-state reference tracking error [42]. Comparing Figs. 3 and 4, it can be observed that $\boldsymbol{k}_{\mathrm{t}} = \boldsymbol{k}_{\mathrm{ti}}$, $F_{\mathrm{i}}(z) = \boldsymbol{k}_{\mathrm{ii}}/(z-1)$, and $\mathbf{C}_{\mathrm{i}}(z) = \mathbf{K}_{\mathrm{i}}$. The closed-loop poles for the inner loop are selected as

$$\boldsymbol{p}_1 = 0 \qquad \boldsymbol{p}_{2,3} = \exp(-\alpha_{\mathrm{c}}T_{\mathrm{s}}) \tag{9}$$

where α_{c} is the desired closed-loop bandwidth and T_{s} is the sampling period. The state-feedback gains and the integral gain are then solved using direct pole placement [39], [40] by writing them in closed form as functions of the system parameters and the desired closed-loop pole locations $\boldsymbol{p}_1, \boldsymbol{p}_2$, and $\boldsymbol{p}_3$. This yields

$$\begin{aligned}
\boldsymbol{k}_1 &= \boldsymbol{\gamma}^{-1}\left(\boldsymbol{p}_1\boldsymbol{p}_2 + \boldsymbol{p}_1\boldsymbol{p}_3 + \boldsymbol{p}_2\boldsymbol{p}_3 + \boldsymbol{k}_2\boldsymbol{\phi} + \boldsymbol{k}_2 - \boldsymbol{\phi}\right) \\
\boldsymbol{k}_2 &= -\boldsymbol{p}_1 - \boldsymbol{p}_2 - \boldsymbol{p}_3 + \boldsymbol{\phi} + 1 \\
\boldsymbol{k}_{\mathrm{ii}} &= \boldsymbol{\gamma}^{-1}\left(-\boldsymbol{p}_1\boldsymbol{p}_2\boldsymbol{p}_3 + \boldsymbol{k}_1\boldsymbol{\gamma} - \boldsymbol{k}_2\boldsymbol{\phi}\right).
\end{aligned} \tag{10}$$

The reference feedforward zero is placed at $\boldsymbol{p}_3$ by selecting the reference feedforward gain as

$$\boldsymbol{k}_{\mathrm{ti}} = \frac{\boldsymbol{k}_{\mathrm{ii}}}{1 - \boldsymbol{p}_3}. \tag{11}$$

The design objective behind this pole and zero parameterization is to achieve first-order reference-tracking dynamics with bandwidth α_{c} under the assumption of purely inductive plant. This results in a rise time from 10% to 90% of $t_{\mathrm{ri}} = 2.2/\alpha_{\mathrm{c}}$ for the reference tracking dynamics. Naturally, the realized bandwidth is lower due to the filter capacitor and the actual load.

Remark 2: The type of the inner-loop controller does not have to match that of the outer voltage controller. If the sole requirement for the inner current loop is the provision of overcurrent protection, e.g., a simple PI-type controller could be employed instead.

B. Outer Voltage Loop

The voltage controller design is based on the assumption of an LC filter plant defined by (25) in the Appendix. In accordance with Fig. 4, the control law for the outer voltage loop becomes

$$\boldsymbol{u}'_{\mathrm{c,ref}}(k) = \boldsymbol{k}_{\mathrm{tu}}\boldsymbol{u}_{\mathrm{f,ref}}(k) + \boldsymbol{u}_{\mathrm{iu}}(k) - \mathbf{K}_{\mathrm{u}}\mathbf{x}^{\mathrm{LC}}(k) \tag{12}$$

$$\boldsymbol{u}_{\mathrm{iu}}(k+1) = \boldsymbol{u}_{\mathrm{iu}}(k) + \boldsymbol{k}_{\mathrm{iu}}[\boldsymbol{u}_{\mathrm{f,ref}}(k) - \boldsymbol{u}_{\mathrm{f}}(k)] \tag{13}$$

where $\boldsymbol{k}_{\mathrm{tu}}$ is the reference feedforward gain, $\boldsymbol{u}_{\mathrm{iu}}$ is the integral state, $\mathbf{K}_{\mathrm{u}}$ is the state-feedback gain vector, and $\boldsymbol{k}_{\mathrm{iu}}$ is the integral gain. Comparing Figs. 3 and 4, it can be observed that $F_{\mathrm{u}}(z) = \boldsymbol{k}_{\mathrm{tu}} + \boldsymbol{k}_{\mathrm{iu}}/(z-1)$, $\mathbf{C}_{\mathrm{u}}(z) = \mathbf{K}_{\mathrm{u}} - \boldsymbol{k}_{\mathrm{tu}}\mathbf{C}_{\mathrm{f}}$, and $H_{\mathrm{u}}(z) = 0$. The closed-loop poles are selected according to [14] as

$$\begin{aligned}
\boldsymbol{p}_{1\mathrm{u}} &= 0 \\
\boldsymbol{p}_{2\mathrm{u}} &= \exp(-(\omega_{\mathrm{r}} - \omega_{\mathrm{g}})T_{\mathrm{s}}) \\
\boldsymbol{p}_{3\mathrm{u},4\mathrm{u}} &= \exp\left[(-\zeta_{\mathrm{r}} \pm j\sqrt{1-\zeta_{\mathrm{r}}^2})(\omega_{\mathrm{r}} - \omega_{\mathrm{g}})T_{\mathrm{s}}\right]
\end{aligned} \tag{14}$$

where ω_{g} is the angular frequency of the synchronous coordinate frame and ζ_{r} is the damping ratio of the resonant pole pair. The state-feedback gains in $\mathbf{K}_{\mathrm{u}}$ and the integral gain $\boldsymbol{k}_{\mathrm{iu}}$ can then be solved by using direct pole placement [14]. The reference feedforward zero is placed at $\boldsymbol{p}_{2\mathrm{u}}$ by selecting the reference feedforward gain as

$$\boldsymbol{k}_{\mathrm{tu}} = \frac{\boldsymbol{k}_{\mathrm{iu}}}{1 - \boldsymbol{p}_{2\mathrm{u}}}. \tag{15}$$

This choice of poles and feedforward zero results in an approximate rise time from 10 to 90% of $t_{\mathrm{ru}} = 1.8/(\omega_{\mathrm{r}} - \omega_{\mathrm{g}})$ for the

reference tracking dynamics [42]. The resulting pole placement is based on the radial projection of the resonant pole pair to damp the *LC* resonance [42]. The two other poles are placed on the real axis: one in the origin and one at the resonance frequency, where the feedforward zero is also placed. For a detailed analysis of the voltage controller, the interested reader is referred to [14].

C. Limiters and Mode Changing

For this example, the instantaneous limiting function is used to limit the amplitude of the current reference [26], [29]. The instantaneous limiting function is defined as

$$\boldsymbol{i}_{\mathrm{c,ref}} = \mathrm{Lim}(\bar{\boldsymbol{i}}_{\mathrm{c,ref}}, i_{\mathrm{c,lim}}) = \begin{cases} \bar{\boldsymbol{i}}_{\mathrm{c,ref}} & \text{if } |\bar{\boldsymbol{i}}_{\mathrm{c,ref}}| \leq i_{\mathrm{c,lim}} \\ \frac{\bar{\boldsymbol{i}}_{\mathrm{c,ref}}}{|\bar{\boldsymbol{i}}_{\mathrm{c,ref}}|} i_{\mathrm{c,lim}} & \text{else.} \end{cases} \tag{16}$$

Additionally, the realizable converter voltage reference is limited by the finite dc-link voltage. This physical limitation is realized in the controller by a limiter function block at the output of the inner current controller, cf. Fig. 4. Typically the limit is chosen either as voltage hexagon formed by the possible output voltage vectors of the converter or as an instantaneous amplitude limiter, cf. (16).

In order to prevent integrator windup in the control loops due to reference saturation, a realizable reference antiwindup is employed [35]. This antiwindup is shown with dashed lines in Fig. 4 for both control loops. Due to the scaling of the signal by $\boldsymbol{k}_{\mathrm{ti}}^{-1}$ before the converter current reference limiter in the proposed cascade structure, additional gain $\boldsymbol{k}_{\mathrm{ti}}$ has to be included in the antiwindup path of the voltage integrator, as depicted in Fig. 4.

The two antiwindups in Fig. 4 maintain proper integral states in the controllers automatically during all modes of operation, excluding the externally set current control mode. In this case, the integral state of the voltage controller tends to drift to a limit set by the converter current reference limiter. This is a consequence of the capacitor voltage reference not being tracked, causing a nonzero input to the integrator. While a typical solution is to freeze the integrator, a seamless transition back to voltage control mode can be achieved by updating the voltage integrator state using the control law [cf. (12)] including the decoupling feedback, and solving it for the integral state. Consequently, the voltage integrator is updated using

$$\begin{aligned} \boldsymbol{u}_{\mathrm{iu}}(k) = {} & \boldsymbol{k}_{\mathrm{ti}} \boldsymbol{i}_{\mathrm{c,ref}}^{\mathrm{ext}}(k) - \boldsymbol{k}_{\mathrm{tu}} \boldsymbol{u}_{\mathrm{f,ref}}(k) + \boldsymbol{u}_{\mathrm{ii}}(k) \\ & + (\mathbf{K}_{\mathrm{u}} - \mathbf{K}_{\mathrm{i}}) \mathbf{x}^{\mathrm{LC}}(k) \end{aligned} \tag{17}$$

while the converter operates in the externally set current control mode. This enables a seamless transition back to voltage control mode.

V. Results

A. Test Setup

The properties of the proposed cascade structure are validated by means of experiments using a 50-Hz 10-kVA three-phase VSC system. In the experiments, the example cascade controller of Section IV is compared to the corresponding single-loop voltage controller based on [14]. The nominal parameters of the system are given in Table I. The base values of the system are based on the values u_{g} and i_{n}.

TABLE I
Nominal Parameters of the Converter System

Parameter	Value	Parameter	Value
u_{g}	$\sqrt{2/3} \cdot 400$ V (1 p.u.)	L_{f}	2.8 mH (0.055 p.u.)
ω_{g}	$2\pi \cdot 50 \frac{\mathrm{rad}}{\mathrm{s}}$ (1 p.u.)	C_{f}	15 μF (0.076 p.u.)
$f_{\mathrm{s}} = f_{\mathrm{sw}}$	8 kHz (160 p.u.)	u_{dc}	650 V (2 p.u.)
i_{n}	$\sqrt{2} \cdot 14.4$ A (1 p.u.)	$i_{\mathrm{c,lim}}$	$1.2 \cdot i_{\mathrm{n}}$ (1.2 p.u.)

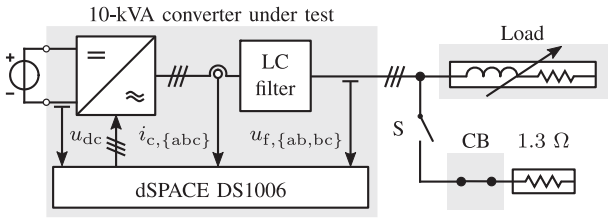

Fig. 5. Block diagram of the experimental setup. CB stands for CB.

The inner current controller bandwidth is $\alpha_{\mathrm{c}} = 2\pi \cdot 1200$ rad/s and the outer voltage controller damping ratio is $\zeta_{\mathrm{r}} = 0.7$. The current controller gains $\mathbf{K}_{\mathrm{i}}$ and $\boldsymbol{k}_{\mathrm{ii}}$ are solved[3] from (10) using direct pole placement and the reference feedforward zero $\boldsymbol{k}_{\mathrm{ti}}$ is solved from (11). Similarly, the voltage controller gains $\mathbf{K}_{\mathrm{u}}$ and $\boldsymbol{k}_{\mathrm{iu}}$ are solved[4] by employing direct pole placement and the reference feedforward gain $\boldsymbol{k}_{\mathrm{tu}}$ is solved using (15), according to [14]. The gains $\mathbf{K}_{\mathrm{u}}$, $\boldsymbol{k}_{\mathrm{iu}}$, and $\boldsymbol{k}_{\mathrm{tu}}$ are used in both the voltage controller of the proposed cascade controller and the corresponding single-loop voltage controller. The voltage-angle generator for the control system in the experiments is based on integrating a constant angular frequency of $\omega_{\mathrm{g}} = 2\pi \cdot 50$ rad/s and employing the resulting angle in the coordinate transforms. The current limit is set as 1.2 times the nominal current of the converter under test, i.e., $i_{\mathrm{c,lim}} = 1.2 \cdot i_{\mathrm{n}}$ (cf. Table I).

A block diagram depicting the experimental setup is given in Fig. 5. A dSPACE DS1106 is used as the platform for implementing the control algorithms on. The converter under test controls only the ac-side quantities, i.e., voltage or current, while another back-to-back converter provides regulation of the dc-link voltage. The converter under test is connected to a variable inductive–resistive load in order to emulate different load conditions. In addition, a CB and a 1.3 Ω (0.08 p.u.) fault-emulating resistance is connected through switch S in parallel with the adjustable load. Unless otherwise stated, the switch S is kept open.

B. Stability Maps

The proposed cascade controller structure is experimentally validated below by using inductive–resistive loads, as such

[3]The resulting gains are $\mathbf{K}_{\mathrm{i}} = [35.664 - 0.552j, 1.220 - 0.039j]$, $\boldsymbol{k}_{\mathrm{ii}} = 8.338 + 0.328j$ and $\boldsymbol{k}_{\mathrm{ti}} = 13.661 + 0.537j$.

[4]The resulting gains are $\mathbf{K}_{\mathrm{u}} = [18.228 - 1.429j, -0.182 + 0.040j, 0.844 - 0.064j]$, $\boldsymbol{k}_{\mathrm{iu}} = 0.262 + 0.015j$, and $\boldsymbol{k}_{\mathrm{tu}} = 0.602 + 0.036j$.

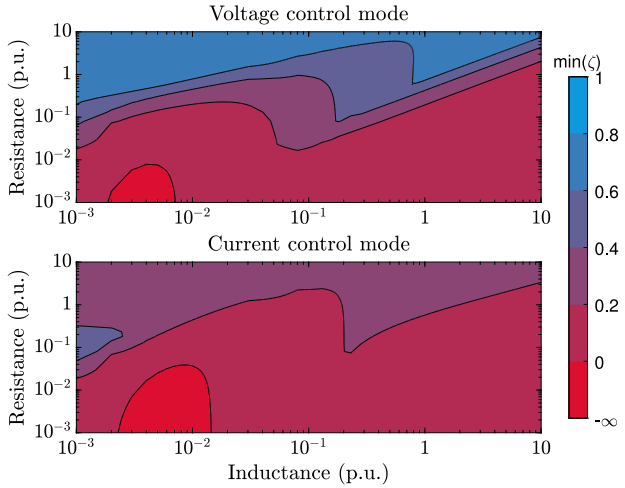

Fig. 6. Stability maps for voltage (top) and current (bottom) control modes of the example controller. The maps show the lowest damping ratio of the closed-loop system for a given inductive–resistive load.

loads are commonly encountered in, e.g., grid applications. To demonstrate the robustness of the employed example controllers to such loads, stability maps that illustrate the lowest damping ratio of the closed-loop system for a given inductive–resistive load are given in Fig. 6. These maps are purely defined by the voltage and current controllers, i.e., the proposed cascade controller structure does not have an effect on the stability of the control modes. The system parameter values and controller gains used in the plotting of the maps are given in Table I and Footnotes 3 and 4 of Section V-A, respectively.

As can be observed, both of the control modes are stable for a wide range of inductance and resistance values. Only a small unstable area can be found in the examined range for relatively low values of inductance, around $[0.002, 0.02]$ p.u., and resistance, around $[0.001, 0.02]$ p.u., for both control modes. The size of this unstable area can be reduced in addition to improving the overall damping ratios at the cost of reducing the bandwidth targets of the controller, i.e., the control designer has to make a tradeoff between the dynamic performance and the robustness to load variations.

C. Experimental Results

1) Dynamic Performance in Voltage Control Mode: First, the dynamic performance of the controllers is compared in order to verify that the proposed cascade structure does not affect voltage control properties under normal operation. The experimental result of this test is shown in Fig. 7. The figure shows the reference tracking performance under no load (left) and under 1 p.u. resistive and 0.45 p.u. inductive load (middle), when a 1 p.u. reference step is applied to the d-axis voltage. Similar responses are obtained for q-axis reference changes. Furthermore, the response to a stepwise change from no-load to 1 p.u. resistive and 0.45 p.u. inductive load during steady-state operation with 1 p.u. d-axis voltage reference is presented (right) to demonstrate the disturbance rejection performance. As can be observed, the dynamic performance of the single-loop voltage controller is not affected by the proposed cascade controller structure under normal operating conditions.

2) Transitioning Between Control Modes: Following the dynamic performance tests, the capability of the proposed cascade structure to manually transition between voltage and current control modes is examined. The transition is triggered by an external mode-select signal set by the user (cf. Fig. 4). Fig. 8(a) and (b) shows the experimental results for transitioning between the control modes for two different loads: 1 p.u. resistive and 0.45 p.u. inductive; and 0.08 p.u. resistive and 0.45 p.u. inductive. The events in the figures unfold as follows. Initially, the converter is operating in voltage control mode. The control mode is then switched to current control while retaining the same operating point. In current control mode, the current reference is set to 0.5 p.u. d-axis current in Fig. 8(a) and to -1 p.u. q-axis current in Fig. 8(b), which changes the operating point of the converter. After this, the control mode is switched back to voltage control mode while retaining the same operating point. Lastly, the operating point is restored to its initial value in voltage control mode. As can be observed in both figures, the transitions between voltage and current control modes occur seamlessly. It is worth noting that the seamless transition from current control to voltage control mode is due to dynamically adjusting the outer voltage loop integrator using (17) while in current control mode.

The transients related to the reference changes in current and voltage control modes are purely determined by the current and voltage controllers, respectively. In Fig. 8(b), the oscillating modes following a reference step in both current and voltage control mode decay in slightly over one period of the oscillating mode's frequency. This result is in line with the stability maps of Fig. 6, which show that the lowest damping ratio for both control modes is around 0.2 for the examined load.

3) Overcurrent Protection: Lastly, overcurrent protection capabilities under fault conditions are examined. As the fault behavior of the proposed cascade structure can be designed flexibly through the choice of the limiting function and both the current and the voltage controllers, the results shown for the application example of Section IV only exemplify the potential of the proposed cascade structure. For comparison, the current limiting method suggested in [14], which is based on the method proposed in [24], is used as a reference. The overcurrent limit of the reference method is set equal to that of the cascade controller, i.e., $1.2 \cdot i_{\mathrm{n}}$. In addition, a case where the converter is designed to trip (as in [12]) in the event of overcurrent is considered as well. A fault is emulated by connecting a 1.3 Ω resistance (0.08 p.u.) in parallel with the steady-state load through switch S (cf. Fig. 5). This fault-emulating load is equipped with a CB that disconnects the fault from the rest of the system in a timely manner.

Fig. 9 shows the experimental results for the fault emulation tests. Initially, the converter is operating with 1 p.u. d-axis voltage reference and 4.7 p.u. resistive and 0.45 p.u. inductive load. Switch S is then closed at $t = 5$ ms, emulating a fault in the load. The leftmost plots show the case of the converter tripping to excessive currents following the fault instant. On the other hand, the reference method [14] (middle plots) starts limiting

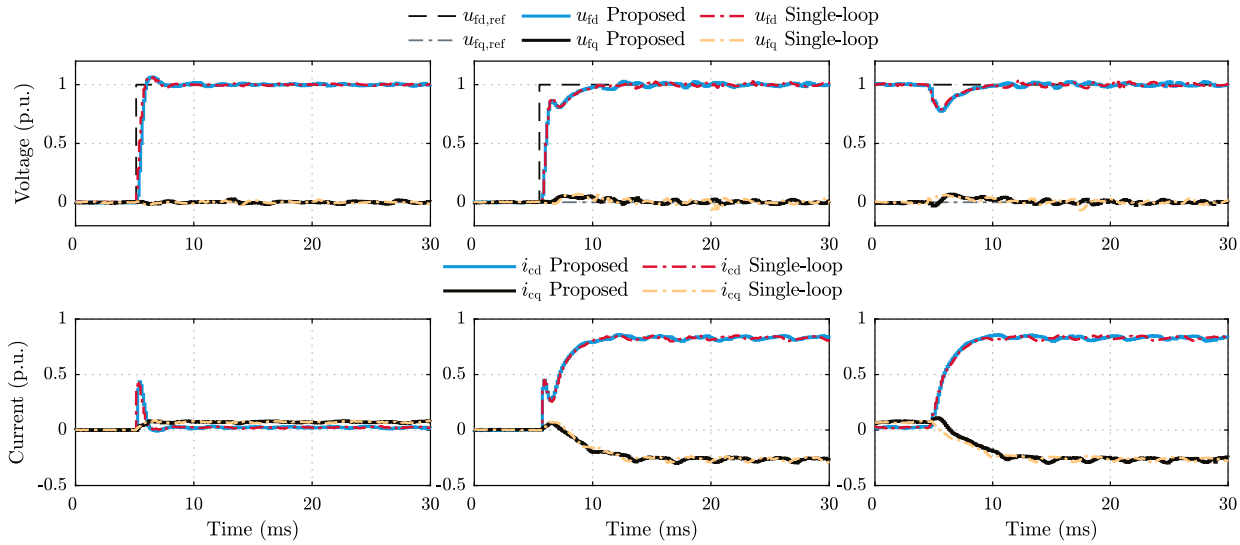

Fig. 7. Experimental validation of the transparency of the current controller in the proposed cascade controller structure. The application example controller presented in Section IV is compared with its single-loop counterpart based on the controller proposed in [14]: (left) reference tracking under no load (middle) reference tracking under 1 p.u. resistive and 0.45 p.u. inductive load and (right) disturbance rejection in the form of load change from no load to 1 p.u. resistive and 0.45 p.u. inductive load.

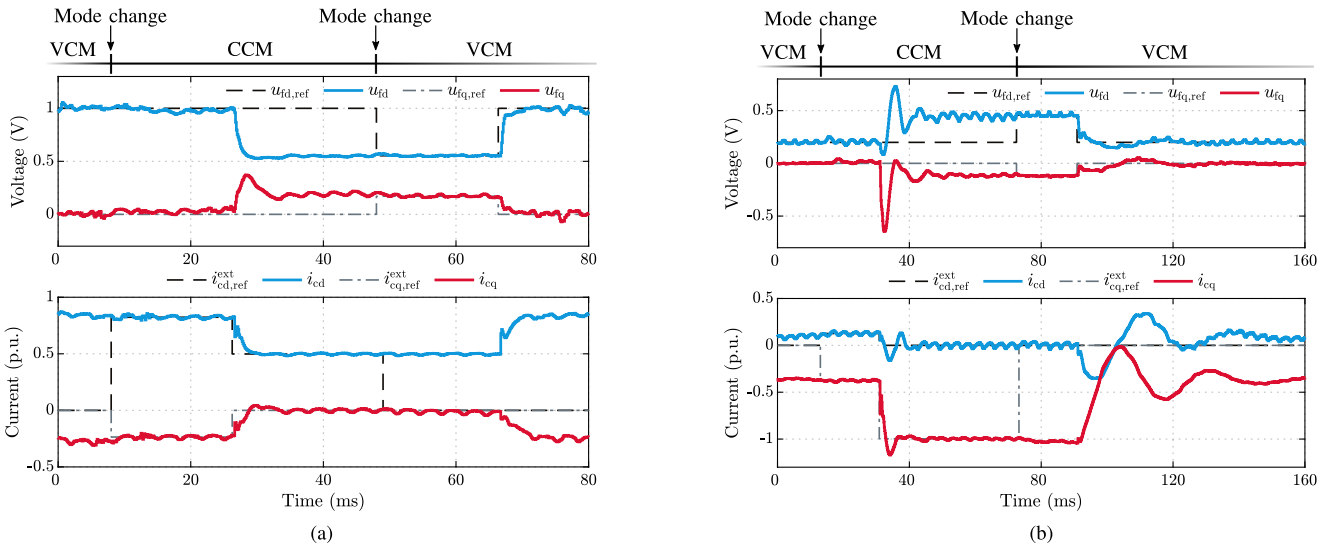

Fig. 8. Experimental transition between control modes with (a) 1 p.u. resistive and 0.45 p.u. inductive load (b) 0.08 p.u. resistive and 0.45 p.u. inductive load. Additionally, reference steps in both control modes are presented. VCM and CCM stand for voltage and current control mode, respectively.

the converter voltage reference to limit the converter current magnitude, and the proposed cascade structure (rightmost plots) automatically transitions into current control mode. The responses of these two cases are relatively similar, although the reference method does not limit the current accurately. Shortly after the occurence of the fault, the CB in the fault-emulating load operates, disconnecting the fault from the system. This causes the cascade controller to transition back to voltage control mode and ends the converter voltage reference limiting in the reference method. It should be emphasized that the transient following the fault clearance is dominated by the CB and not the controllers.

While the reference method successfully limits the current, it was found sensitive to assumptions regarding equivalent losses in the filter inductor and the converter, which easily results in inaccurate limitation. Furthermore, the reference method was found to have an adverse effect on the dynamic performance of the voltage controller in addition to requiring measurements of the load current $\boldsymbol{i}_{\mathrm{o}}$. On the contrary, overcurrent protection capability comparable to the reference method can be achieved with the proposed cascade controller structure while limiting the converter current accurately even under modeling errors and without affecting the dynamic performance under linear operation.

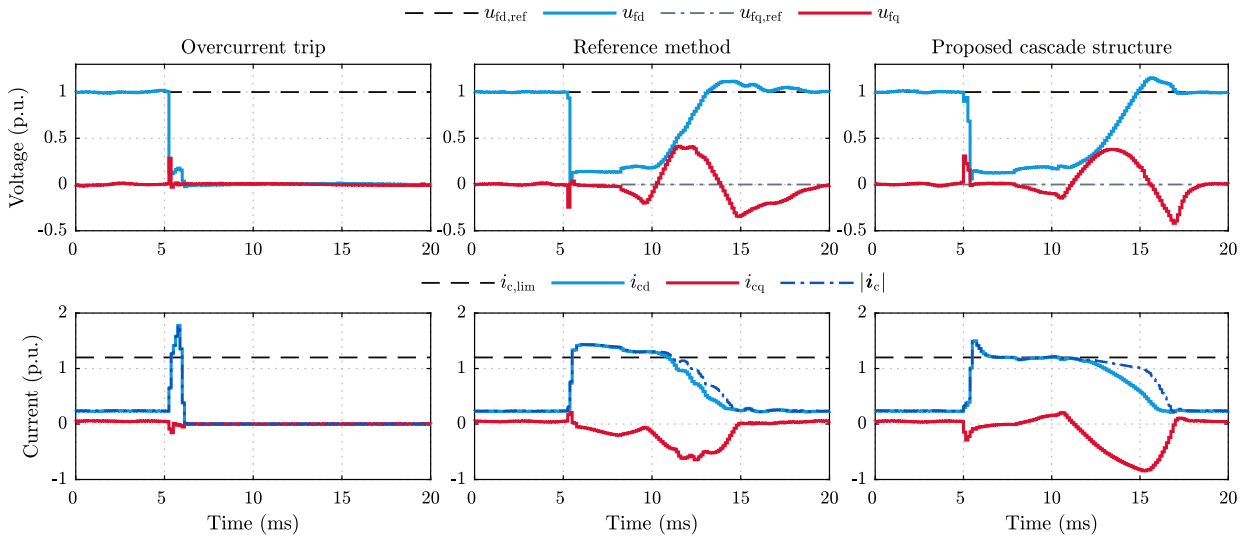

Fig. 9. Experimental emulation of a load fault by connecting a low-resistance load in parallel with the steady-state load. Recovery from the fault, which is triggered by a CB, is also shown. The fault emulation is shown for the case where the converter is designed to trip in the event of overcurrent (left), for the reference current limitation method suggested in [14] (middle), and for the proposed structure (right).

VI. Conclusion

This article presented a multifunctional cascade controller structure for VSCs. The proposed controller structure allows for operation in either voltage or current control mode. In voltage control mode and under linear operation, the current controller can be made completely transparent. Consequently, the properties of both control modes are purely determined by their corresponding control loops, which can be designed independently of each other. The transitions between control modes are seamless and occur either due to converter overloading, i.e., the controller inherently includes overcurrent protection, or by manually activating the current control mode of the controller. The properties of the proposed cascade controller structure were validated by means of experiments.

Appendix
Discrete-Time Models of the L and LC Filters

In formulating the hold-equivalent models of the L and LC filters, the model inputs are assumed to be modeled as zero-order hold in stationary coordinates for simplicity. Furthermore, sampling of the converter currents and capacitor voltages is assumed to be synchronized with the PWM.

A. Hold-Equivalent Model of the L Filter

The L filter model consists of an inductance L_{f} and a resistance R_{f}, i.e., the first row of (1). From the continuous-time model, the hold-equivalent model of the L filter in synchronous coordinates can be obtained as [43]

$$\boldsymbol{i}_{\mathrm{c}}(k+1) = \boldsymbol{\phi}\boldsymbol{i}_{\mathrm{c}}(k) + \boldsymbol{\gamma}\boldsymbol{u}_{\mathrm{c}}(k) - \boldsymbol{\gamma}\boldsymbol{u}_{\mathrm{f}}(k) \tag{18}$$

where

$$\boldsymbol{\phi} = \boldsymbol{\delta}e^{-\frac{R_{\mathrm{f}}}{L_{\mathrm{f}}}T_{\mathrm{s}}} \qquad \boldsymbol{\gamma} = \frac{\boldsymbol{\delta}-\boldsymbol{\phi}}{R_{\mathrm{f}}} \qquad \boldsymbol{\delta} = e^{-j\omega_{\mathrm{g}}T_{\mathrm{s}}}. \tag{19}$$

Due to the finite computational time of the control system, one-sample delay in realizing the converter voltage reference is included in the model, i.e.,

$$\boldsymbol{u}_{\mathrm{c}}(k+1) = \boldsymbol{\delta}\boldsymbol{u}_{\mathrm{c,ref}}(k). \tag{20}$$

This computational delay can be augmented into the hold-equivalent L filter model (18) as

$$\mathbf{x}^{\mathrm{L}}(k+1) = \begin{bmatrix}\boldsymbol{\phi} & \boldsymbol{\gamma}\\ 0 & 0\end{bmatrix}\mathbf{x}^{\mathrm{L}}(k) + \begin{bmatrix}0\\ \boldsymbol{\delta}\end{bmatrix}\boldsymbol{u}_{\mathrm{c,ref}}(k) - \begin{bmatrix}\boldsymbol{\gamma}\\ 0\end{bmatrix}\boldsymbol{u}_{\mathrm{f}}(k) \tag{21}$$

where $\mathbf{x}^{\mathrm{L}} = [\boldsymbol{i}_{\mathrm{c}}, \boldsymbol{u}_{\mathrm{c}}]^{\mathrm{T}}$.

B. Hold-Equivalent Model of the LC Filter

The continuous-time LC filter model in stationary coordinates is defined by (1). An ideal filter is assumed, i.e., $R_{\mathrm{f}} = 0\,\Omega$. Based on the ideal continuous-time model, the hold-equivalent model of the LC filter in synchronous coordinates rotating at ω_{g} can be written as

$$\mathbf{x}(k+1) = \boldsymbol{\Phi}\mathbf{x}(k) + \boldsymbol{\Gamma}_{\mathrm{c}}\boldsymbol{u}_{\mathrm{c}}(k) + \boldsymbol{\Gamma}_{\mathrm{o}}\boldsymbol{i}_{\mathrm{o}}(k) \tag{22}$$

where the system matrix $\boldsymbol{\Phi}$ and the vectors $\boldsymbol{\Gamma}_{\mathrm{c}}$ and $\boldsymbol{\Gamma}_{\mathrm{o}}$ are obtained from

$$\begin{aligned}\boldsymbol{\Phi} &= \boldsymbol{\delta}e^{\mathbf{A}T_{\mathrm{s}}} \quad \boldsymbol{\Gamma}_{\mathrm{c}} = \boldsymbol{\delta}\left(\int_0^{T_{\mathrm{s}}} e^{\mathbf{A}\tau}d\tau\right)\mathbf{B}_{\mathrm{c}}\\ \boldsymbol{\Gamma}_{\mathrm{o}} &= \boldsymbol{\delta}\left(\int_0^{T_{\mathrm{s}}} e^{\mathbf{A}\tau}d\tau\right)\mathbf{B}_{\mathrm{o}}\end{aligned} \tag{23}$$

as

$$\boldsymbol{\Phi} = \boldsymbol{\delta}\begin{bmatrix} \cos(\omega_\mathrm{r} T_\mathrm{s}) & -\frac{\sin(\omega_\mathrm{r} T_\mathrm{s})}{\omega_\mathrm{r} L_\mathrm{f}} \\ \sin(\omega_\mathrm{r} T_\mathrm{s})\omega_\mathrm{r} L_\mathrm{f} & \cos(\omega_\mathrm{r} T_\mathrm{s}) \end{bmatrix}$$
$$\boldsymbol{\Gamma}_\mathrm{c} = \boldsymbol{\delta}\begin{bmatrix} \frac{\sin(\omega_\mathrm{r} T_\mathrm{s})}{\omega_\mathrm{r} L_\mathrm{f}} \\ 1-\cos(\omega_\mathrm{r} T_\mathrm{s}) \end{bmatrix} \quad \boldsymbol{\Gamma}_\mathrm{o} = \boldsymbol{\delta}\begin{bmatrix} 1-\cos(\omega_\mathrm{r} T_\mathrm{s}) \\ -\frac{\sin(\omega_\mathrm{r} T_\mathrm{s})}{\omega_\mathrm{r} C_\mathrm{f}} \end{bmatrix}. \tag{24}$$

As with the hold-equivalent L filter model, the hold-equivalent LC filter model (22) is augmented with the computational delay state (20) as

$$\mathbf{x}^{\mathrm{LC}}(k+1) = \begin{bmatrix} \boldsymbol{\Phi} & \boldsymbol{\Gamma}_\mathrm{c} \\ \mathbf{0} & 0 \end{bmatrix} \mathbf{x}^{\mathrm{LC}}(k) + \begin{bmatrix} \mathbf{0} \\ \boldsymbol{\delta} \end{bmatrix} \boldsymbol{u}_{\mathrm{c,ref}}(k) + \begin{bmatrix} \boldsymbol{\Gamma}_\mathrm{o} \\ 0 \end{bmatrix} \boldsymbol{i}_\mathrm{o}(k) \tag{25}$$

where $\mathbf{x}^{\mathrm{LC}} = [\mathbf{x}, \boldsymbol{u}_\mathrm{c}]^\mathrm{T}$.

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