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Fully Digital On-Chip Wideband Background Calibration for Channel Mismatches in Time-Interleaved Time-Based ADCs

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Abstract—This letter presents a fully integrated on-chip digital mismatch compensation system for time-based time-interleaved (TI) data converters. The proposed digital compensation features blind calibration of gain, offset, and timing mismatches. The implemented system uses time-based sampling clock mismatch detection, achieving convergence within 32K samples, which is on par with analog-assisted background methods. A specialized filter structure compensates for timing mismatches of magnitude up to 0.21 of the sampling period, nearly triple the range of other published digital compensation methods, and is effective for input signals up to 0.92 Nyquist bandwidth. The on-chip digital correction achieves suppression of all mismatch tones to levels below -60 dBc while running fully in the background. The operation is demonstrated with an $8 \times$ TI 2-GS/s analog-to-digital converter (ADC) prototype chip implemented in a 28-nm CMOS process.

Index Terms—Analog-to-digital converter (ADC), cyclic-coupled ring oscillator (CCRO), digital calibration, finite-impulse response (FIR), least mean-square (LMS), mismatch, time based, time interleaving, timing skew.

I. INTRODUCTION

Modern wireless communication applications require analog-to-digital converters (ADCs) with gigahertz-range bandwidth (BW). The time-interleaved (TI) ADC is a common architecture for achieving a wideband operation by carrying out the conversion with several parallel sub-ADCs. However, the overall performance of the TI-ADC is limited by the matching between the sub-ADCs in terms of gain, offset, and timing. The mismatches can be detected and corrected in analog, digital, or mixed-signal domains. Analog-assisted digital methods can provide a fast and accurate calibration for the mismatch errors. However, they require auxiliary circuits [1], [2] or reference ADCs. Split TI-ADC is proposed for reference-free calibration [3]. Fully digital methods [4] can provide more general and flexible solutions that are portable between process nodes and designs.

This letter presents a fully integrated on-chip digital mismatch compensation solution with a unique background skew correction scheme facilitated by the time-based converter architecture. It employs a least mean-square (LMS) algorithm for blind gain and offset calibration and a fully digital skew mismatch estimator, achieving convergence within 32K samples, which is comparable to other analog-assisted methods. Furthermore, a cascaded reconstruction filter structure is implemented to compensate for timing mismatches of magnitude up to $0.21 T_s$, providing nearly triple the range of other compensation methods while retaining a wide $0.92 f_{Nyq}$ correction BW. The proposed digital calibration system aims to ease the complexity of analog front-end design in terms of matching and clock distribution.

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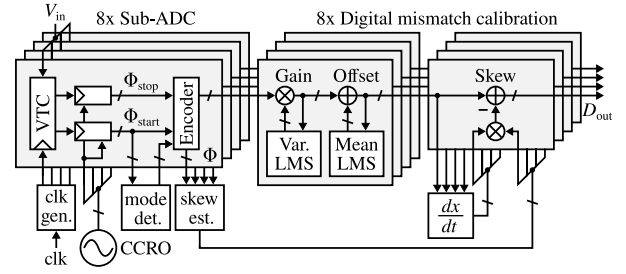


Fig. 1. Block diagram of the time-based $8 \times$ TI ADC with inherent time-based skew estimation and on-chip digital mismatch calibration for gain, offset, and timing mismatches.

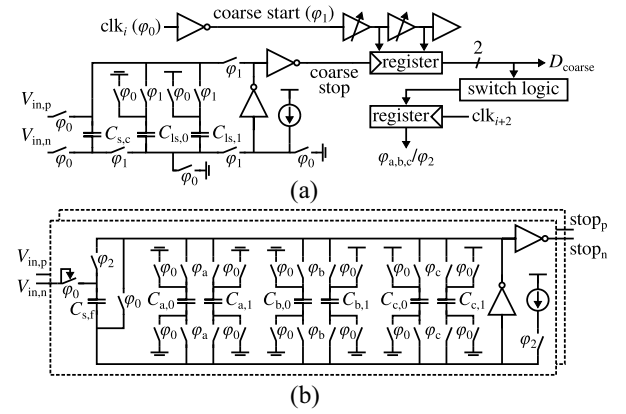


Fig. 2. Constant-slope VTC, with (a) coarse VTC and TDC and (b) pseudodifferential fine VTC.

This letter is organized as follows. Section II presents the time-based TI-ADC architecture. The channel mismatch calibration is described in Section III. Section IV presents the measured results and comparison to comparable works.

II. TIME-BASED TI-ADC

Fig. 1 presents the block diagram of the prototype TI-ADC, where eight time-based 250-MS/s ADCs are time interleaved to operate as a 2-GS/s TI-ADC. The prototype sub-ADC employs a constant-slope voltage-to-time converter (VTC) and a cyclic-coupled ring oscillator (CCRO) time-to-digital converter (TDC). The CCRO TDC and encoder are based on our earlier work [5], [6]. To support the description of the calibration methods used in this letter, the operation of the ADC is briefly described as follows.

Fig. 2 shows the schematic of the coarse-fine VTC (“VTC” in Fig. 1), which converts the input voltage to a time signal used to sample the CCRO. Fig. 2(a) shows the coarse VTC, which resolves 1.5 bits D_{coarse} using a delay line (DL) TDC, and Fig. 2(b) shows the fine VTC schematic. Both VTCs operate by sampling the input voltage to the sampling capacitor and discharging it with a constant

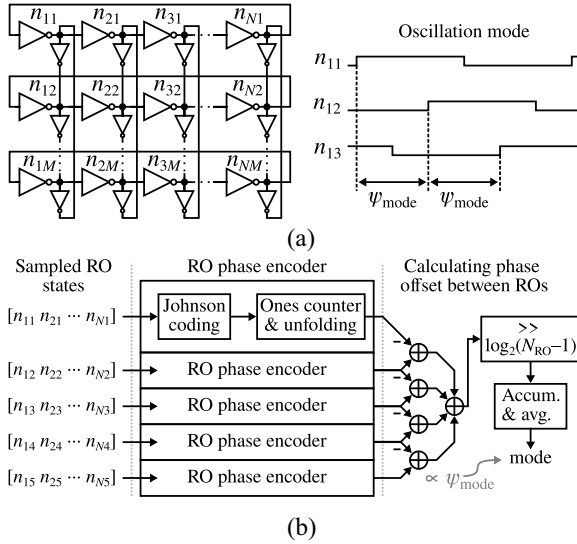


Fig. 3. (a) CCRO schematic and oscillation mode phase offset illustration and (b) on-chip digital CCRO oscillation mode detector based on Johnson coding and ones counting RO encoders.

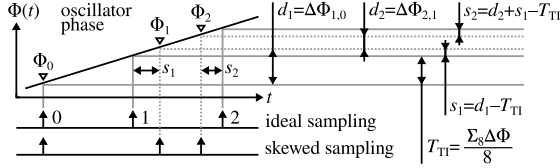


Fig. 4. Estimation of clock skew mismatch from sampled states of the CCRO.

current, which results in a constant-slope voltage ramp. An inverter is used as a comparator to detect the ramp threshold crossing and to generate the stop signal. The sampled voltage is shifted above the comparator threshold using capacitive level shifting in both VTCs. In the coarse VTC, a constant level shift is applied. In the fine VTC, a variable level shift is used with a three-level DAC controlled by φ_a, φ_b , and φ_c derived from D_{coarse} , which implements residue extraction. The nominal resolution of the ADC is close to 10 bits, but the VTC operation is noise limited to approximately 8 bits. The VTC can be operated in a single-ended mode, where stop_n is bypassed with the clock signal, for fixed skew reference described in Section III.

The output time signals of the VTC are used to sample the CCRO in the TDC, which is shared between the TI-ADC channels. $N = 7$ and $M = 11$ CCRO can start in one out of $M - 1$ oscillation modes at startup, which define the order of transitions in the CCRO. The mode must be known in order for the CCRO encoder described in [5] and [6] to function. Hence, a CCRO mode detector (“mode det.” in Fig. 1) is proposed. The schematic of an N -by- M CCRO, and an illustration of the mode-dependent phase offset ψ_{mode} is shown in Fig. 3(a). Fig. 3(b) presents the CCRO mode detector, which calculates the relative phase offset ψ_{mode} between the N_{RO} ring oscillators (ROs) in the CCRO. The instantaneous state of each RO is converted to a binary number, and the differences between adjacent ROs are calculated to get an estimate of the current oscillation mode. The mode detector is run only at chip startup and, hence, its power consumption is negligible.

III. MISMATCH CALIBRATION

In this work, the CCRO time reference is utilized for extracting the skew mismatch information directly from the CCRO samples. Fig. 4 illustrates the principle of the time-based clock skew estimation. The

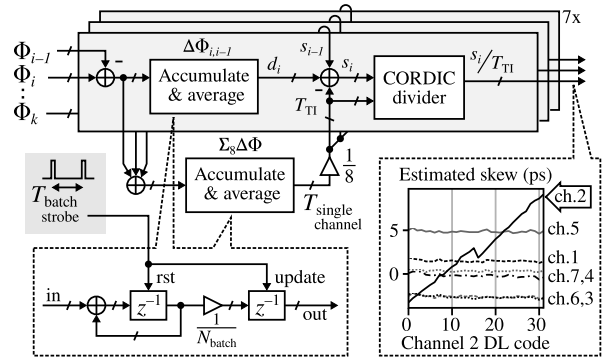


Fig. 5. Block diagram of time-based sampling clock skew estimator. Supplementary chart shows measured skew estimates when the DL in the channel 2 sampling clock path is adjusted.

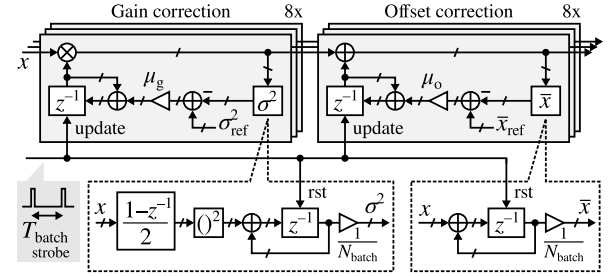


Fig. 6. Implementation of the LMS algorithm for gain and offset correction. Correction factors are updated every T_{batch} , when mismatch corresponding estimators produce a new observation.

linear phase of the oscillator is sampled at nearly uniform intervals at the rising edge of start signals $\Phi_{0:7}$ corresponding to sampling instances of the TI channels. Due to the linearly increasing phase, the calculated phase offsets are proportional to the time intervals between clock sampling instants. Since the start-signal samples are inherent to TDC data conversion, the proposed skew estimator operates with any ADC input and can be run in the background.

The structure of the hardware algorithm is shown in Fig. 5. Up to 32K samples are averaged to suppress noise and improve the estimate precision beyond the time resolution of the CCRO. Skew values relative to the sampling period are obtained from estimates of individual phase differences $\Delta\Phi$ and the TI-ADC period $T_{\text{TI}} = (1/8) \sum_8 \Delta\Phi$ using a CORDIC-based divider. Fig. 5 also shows the measured skew output when the delay of channel 2 sampling clock is adjusted, demonstrating the operation of the estimator. The time resolution of the CCRO changes with PVT corners, which affects the resolution of the skew estimator. However, increasing the averaging depth can compensate this effect. Standard deviation of the estimates observed at 32K averaging is below 200 fs, which compares to ENOB loss of at most 0.2 bits near Nyquist in a 2-GS/s 8-bit $8 \times$ TI-ADC model. The skew estimator consumes 4.7 mW in continuous operation, although it can be duty cycled based on the expected coherence time of the skew parameters.

The digital data correction is performed in three consecutive stages as illustrated in Fig. 1. An LMS algorithm is employed for gain and offset correction, where each ADC channel data path is equipped with a parameter estimator and a feedback path, as shown in Fig. 6. The variance estimator σ^2 used for gain correction consists of high-pass stage $(1 - z^{-1})/2$ and is followed by a squaring operation and a configurable accumulator. This estimator is insensitive to the channel offset and, hence, gain correction is performed first. It is

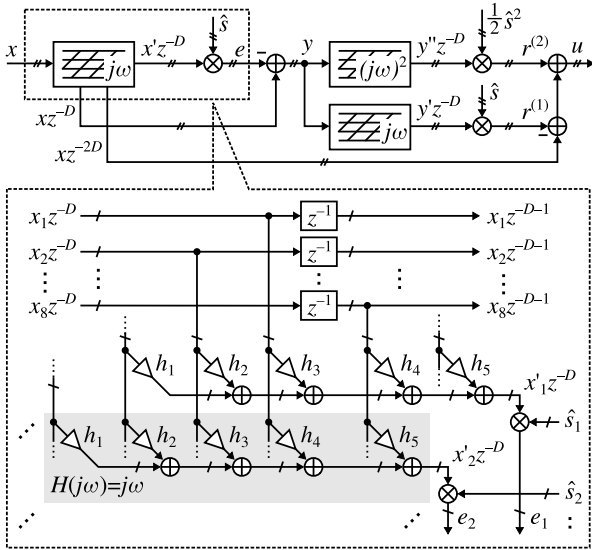


Fig. 7. Structure of filter cascade for timing skew compensation. Each multichannel filter block consists of eight differentiators with their polyphase components distributed across multiple data paths.

then followed by offset correction to eliminate any residual gain-mismatch-dependent offset errors. The offset correction algorithm is structurally similar to the gain correction algorithm; the configurable accumulator is used to estimate channel offset \bar{x} . To reduce the amount of runtime computation, both LMS algorithms operate in the batch mode; the correction of mismatches is executed for each ADC sample, whereas the update of correction factors is done in batches of samples. Each period of T_{batch} , individual channel estimators produce a new output, which is then compared with reference values for gain σ_{ref}^2 and offset \bar{x}_{ref} , and corresponding correction factor accumulators are updated with their weighted difference. The learning rate of each LMS algorithm is controlled with a configurable convergence factor μ . The LMS hardware uses fractional fixed-point arithmetic precision of Q16.24, which delivers correction performance on par with floating-point precision.

The skew correction algorithm employs a 2-stage cascaded filter structure as illustrated in Fig. 7. The first stage produces a preliminary corrected reference signal y from the input signal x and skew estimates, enabling the second stage to achieve more accurate Taylor expansion of the signal y for correcting the original signal x [7]. The 2-stage approach enables a wider range of skew mismatch compensation, up to 21% of the sampling period when applied to the $8 \times$ TI-ADC, as opposed to 4.1% with a single-stage approach as reported in [3] and [4]. In this design, finite-impulse response (FIR) filters of the 64th order are utilized to enable up to $0.92 f_{\text{Nyq}}$ effective skew calibration BW. Each sub-ADC channel has its own cascade configuration, which is split into polyphase components and distributed across the TI data paths as shown in Fig. 7, allowing the digital backend to work at the sub-ADC sample rate of 250 MS/s [8]. The digital compensation system is insensitive to PVT variations.

IV. MEASUREMENT RESULTS

The prototype chip is implemented in a 28-nm CMOS process and wire bonded directly to the measurement PCB. The chip micrograph is shown in Fig. 8, where the ADC core (VTC and TDC) and DSP block (dashed section) occupy an area of 0.24 and 0.92 mm², respectively. Fig. 9(a) and (b) presents the measured single-tone spectra at above $0.9 f_{\text{Nyq}}$ input frequency with and without the digital calibrations. Fig. 9(c) and (d) shows the measured performance and the spur

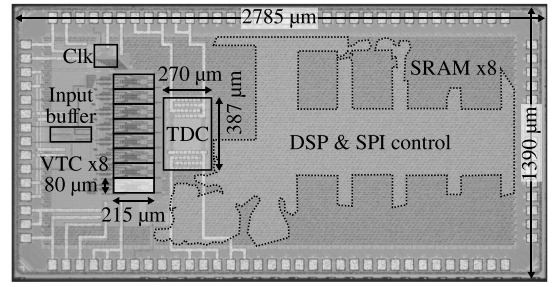


Fig. 8. Chip micrograph.

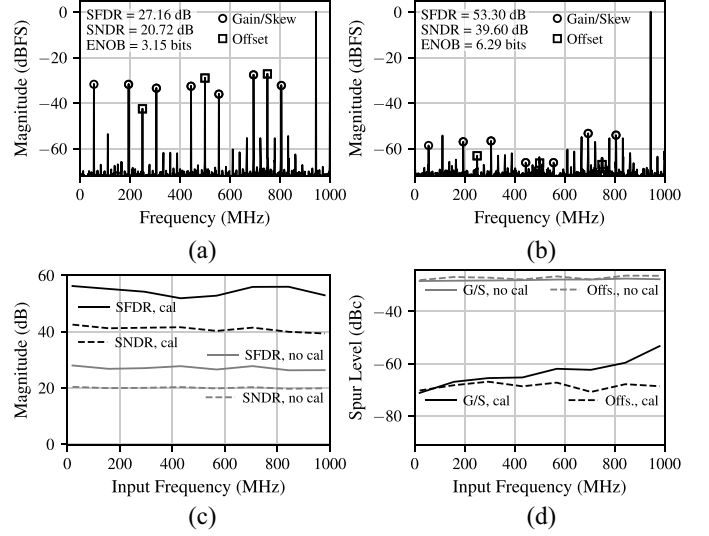


Fig. 9. Measured single tone spectra (a) without and (b) with the proposed calibrations at above $0.9 f_{\text{Nyq}}$ input frequency, and measured (c) performance and (d) mismatch spur level over the input frequency range.

level over the full 1-GHz BW. The initial mismatch of the ADC is large due to the nonmatched current biasing network. Enabling the gain, offset, and skew calibrations improves the SFDR and SNDR by over 30 and 20 dB, respectively. With the calibrations enabled, the ADC maintains SNDR of approximately 40 dB over the full BW. Timing skew mismatch produces the dominant mismatch tones, which remain below -60 dBc until 800 MHz and rise to -53 dBc at Nyquist with 990 MHz input due to the BW limit of the digital filters. A small amount of residual skew mismatch contributes to upward trend in the overall skew spur level. The measured mean ENOB of the sub-ADCs is 6.44 bits at Nyquist, which implies only a 0.15-bit degradation in $8 \times$ TI mode. The TI-ADC (excluding input buffer and clock divider) consumes 48.7 mW from a 0.9-V supply at 2-GS/s sample rate, resulting in a 323-fJ/conv.-step Walden FoM at 990-MHz input. In this proof-of-concept implementation, which is not optimized for power consumption, the digital calibration circuits dissipate 237 mW of power and consist of 342K standard cells, from which approximately 88% is constituted by additional timing closure measures such as optional pipeline registers and the associated clock tree. Although the presented design is targeted at a wide range of channel mismatches, the calibration structure proposed in this work is scalable to different resolution and BW requirements by shrinking the fractional arithmetic part of the LMS algorithm (linear tradeoff) or reducing the length of the FIR filters (logarithmic tradeoff) [7]. Table I compares the performance to recently published state-of-the-art designs.

TABLE I
PERFORMANCE COMPARISON

	This Work	ISSCC'14 [4]	JSSC'17 [2]	JSSC'18 [1]	JSSC'20 [3]
Architecture	8x TI TBADC	12x TI SAR	16x TI SAR	16x TI SAR	7/8x TI SAR
Process (nm)	28	40	40	40	28
Supply (V)	1.8/0.9	1.7/1.1	2.5/1.1	1.1	0.9/0.8
Sample rate (GS/s)	2.0	1.6	2.0	2.6	1.6
SNDR _{Nyq} (dB)	39.3	48	39.4	50.6	54.2
Power (mW)	48.7^a	93.0 ^b	54.2	18.4	12.2
FoM _{W,Nyq} (fJ/c.-s.)	323^a	283 ^b	355	25.6	18.2
Area (mm ²)	0.24^a	0.83 ^b	0.54	0.825	0.078
Full on-chip calibration	Yes	Yes	Yes	No	No
Background	Yes	Yes	No	Yes	Yes
Aux. circuits required	No	No	Yes	Yes	No
Skew estimation	Time-based	Digital slope	Pilot signal + digital logic	Analog delta + digital mixing	Processing split TI data
Skew correction	65-tap FIR 2x	FIR filter	Delay line in clock path	Direct digital interpolation	25-tap FIR + Hilbert
Correction BW (f_{Nyq})	0.92	0.94	1.0	1.0	3.12
Convergence time (kS)	32.8	N/A	10	65.5	80
Skew cal. range (T_s)	0.21^c	0.071 ^c	0.025	0.057	0.041 ^c
Skew cal. range (ps)	106^c	44.4 ^c	12.5	22.0	25.6 ^c
Skew cal. step (fs)	30.6	N/A	400	N/A	N/A

^a VTC & TDC power/area (excluding the digital compensation power).

^b Digital compensation power/area included.

^c Simulated correction range where SNDR is within 3 dB from nominal with a sinusoidal input at 75% Nyquist rate. The skew of a single ADC channel is swept and ideal skew estimation is assumed for correction utilizing reported filter architecture.

V. CONCLUSION

The presented digital calibration system enables blind and standalone on-chip calibration of gain, offset, and timing skew mismatches without the use of any auxiliary circuits, yet exhibiting fast convergence (32K samples) on par with alternative analog-assisted methods. The cascaded reconstruction filter structure implemented on-chip can process wideband signals with frequency up to $0.92 f_{Nyq}$ and address timing skew mismatches up to $0.21 T_s$, which is nearly triple the range of similar reported works. The digital mismatch correction achieves suppression of all interleaving mismatch tones to levels below -60 dBc. The proposed calibration scheme employs digital-intensive and time-based signal processing and is capable of correcting wide range of channel mismatches, which makes it suitable for heavily automated designs.

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