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All-Digital Phase-Locked Loop in 40 nm CMOS for 5.8 Gbps Serial Link Transmitter

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Abstract—This paper describes an all-digital phase-locked loop based clock generator for a MIPI M-PHY serial link transmitter. The paper focuses on ADPLL phase accumulator speed optimization, PVT calibration, loop type changing criteria and power saving in phase digitization process. The experimental circuit is implemented in 40 nm CMOS and generates the MIPI M-PHY defined frequencies from 1.2 GHz to 5.8 GHz.

I. INTRODUCTION

MIPI physical layer (M-PHY) defines a high speed interface for communication between components inside a mobile device. In a low pin count condition, with limited circuit board space a serial bus with multiple transmission speeds is suggested as a suitable solution by MIPI Alliance [1].

We have designed a complete serial link transmitter IC for MIPI M-PHY, as depicted in Fig. 1. Data transmission rates are selected by multiplication factors 1, 2 or 4, whereas digitallycontrolled ring oscillator (DCO) is only meant to produce either 1248 MHz (MIPI A) or 1457.6 MHz (MIPI B) from 19.2 or 26 MHz standard references available on mobile platforms. The overall transmitter has been presented in [2], and the oscillator and multiplier entity in [3], while in this paper we focus on the advanced features in the implemented all-digital phase-locked loop (ADPLL). Section II describes ADPLL digital blocks. The section discusses optimization for speed strategy to enable faster operation of incrementer with standard 40 nm CMOS digital cells. A reliable method to combat PVT variations and reach target output frequency is also detailed in the section. Further we demonstrate a compact and efficient settling monitor governing transition to phase-locking. Section III focuses on custom-designed ADPLL blocks. This section introduces a power saving feature for time-to-digital conversion (TDC) line to conserve energy in mobile devices. Section IV presents measurement results and Section V concludes the paper.

II. DIGITAL BLOCKS OF ADPLL

A. Variable phase accumulator

VPA (marked as Σ in Fig. 1) is employed in ADPLL as output frequency estimator, operating at the highest frequency available on board. It is nevertheless expected to provide extra



Fig. 1. System block diagram of the serial link transmitter.

timing guarantee to function in the worst process and environmental corners. Our proposal for standard-cell incrementer modification to improve speed is outlined in Fig. 2.

To combat summation latency, a single VPA with full wordlength N is divided into ripple-carry sub-accumulators of smaller wordlengths N-R and R working in parallel (transition A in the Fig. 2). In contrast with reference design [4], a new clock domain is added to the incrementer. First, this reduces wordlength of the high-rate sub-accumulator and second, provides flexibility in trade-offs as revealed below.

To entirely eliminate high-rate feedback, LSB of lower-rate sub-accumulator is taken as a feed for a high-rate pipeline utilized in place of high-rate sub-accumulator (transition B in the Fig. 2). From the symmetry of pipeline outputs' bit-patterns one may heuristically construct R levels of XOR chains to

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Fig. 2. Generalized speed enhancement optimization of standard-cell VPA.

compress pipeline outputs' data back to the wordlength of R to complement lower-rate sub-accumulator.

Furthermore, to free the pipeline from any combinational circuits in-between the stages, code transformations are moved to low frequency clock (transition C in Fig. 2). High-rate pipeline can now operate at the highest achievable rate.

An engineering trade-off between degree of pipelining and power consumption is exposed for large R. As R grows, clock distribution network expands, becomes branchy and requires buffers for low clock skew and coherent update of 2^{R} -1 flipflops. Clock buffers toggling at a high rate may raise dynamic power consumption.

The other consideration in proper R selection is sharing $1/2^R$ divider between ADPLL blocks to reduce overall area and dynamic power consumption. In the current implementation N is 8 and we found R=2 to be optimal permitting reuse of 1/4 divider by both VPA and Σ - Δ dithering blocks.

B. Structure of the loops

The goal of variations loop logic (PVT loop part of Fig. 3) is to approach the target output frequency and remain in its vicinity. This is implemented with bisection method as follows. dp step generation circuit is initialized with 2^{P-2} value which



Fig. 3. Combined forward paths of implemented ADPLL.

is then halved in every CKR cycle until the step size of 1LSB. Frequency error sign is constantly monitored to decide whether to add dp_stp or subtract it from dp control of the DCO. When sign monitor captures a change of the frequency error trend, it sets $dp_frz = 1$ to freeze dp control word in its current state. The ADPLL then switches to next loop topology.

Acquisition loop (ACQ loop part of Fig. 3) utilizes PLL type I topology to provide fast dynamics and enable quick transition to the next mode. The transition is governed by settling monitor which locks the condition of stable da control as follows: lower part of the monitor awaits frequency error magnitude fe to be less than integer part of frequency command word (FCW) and activates the other half. The monitor then observes overshoot magnitude on da control to enable LSB pipelining. ADPLL features 7 pipe stages (L) and if da control stabilizes for 8 CKR cycles $da_frz = 1$ initiates transition to tracking.

Tracking loop (TRK loop part of Fig. 3) reflects PLL type II topology and features high order filter to achieve sharp transition to stopband for phase noise reduction. The filter is implemented as a chain of 4 IIR blocks. Simple single-pole IIR blocks exhibit unconditional stability and allow to govern pole location with a single parameter ρ_i . Programmable register regR is provided in the design for storing $\rho_{1...4}$ coefficients.

Considering hardware implementation of ADPLL blocks, one needs to restrict wordlengths. The number N of bits for integer error processing was chosen to cover frequencies ratio

$$N = \left\lceil \log_2 \left(\frac{F_{CKV}}{F_{CKR}} \right) \right\rceil,\tag{1}$$

which for target application is maximized with $F_{CKV} = 1457.6$ MHz and $F_{CKR} = 19.2$ MHz when the ratio is 75.

8 bits are enough to represent the decimal with one bit extra guarantee to allow wider range of reference frequencies.

Bitcount M of fractional error was picked to set accuracy in TDC normalization (outlined as \otimes in Fig. 1) in presence of TDC granularity and decimals truncation. Once F_{CKV} options are specified and TDC line granularity T_{INV} is known from simulations, one can find lower bound for M from inequation

$$\frac{1 - max\{\frac{\Delta T_R}{T_{INV}}\} \times (T_{INV} \times F_{CKV})_M}{F_{CKV}} \le T_{INV}, \quad (2)$$

where $\frac{\Delta T_R}{T_{INV}}$ is integer, reflecting CKV and REF rising edges' time lag in terms of inverter delay, and $(\cdot)_M$ is fractional, representing M-bits approximation of a given fractional number. Equation (2) physically means that M bits permit CKV and REF to be one T_{INV} apart, while more accuracy comes with more bits and averaging (shown as AVG in Fig. 1). In this ADPLL achieved granularity $T_{INV} = 20 \ ps$ and M=8.

C. Gain coefficients

DCO output frequency f_{RG} is a nonlinear function of dp, da and dt controls. In the closed loop operation these controls depend on FCW and with linear Taylor approximation one gets

$$f_{RG}(\widehat{FCW}) \approx f_{RG}(FCW) + f'_{RG}(FCW)(\widehat{FCW} - FCW),$$
(3)

where $\overline{FCW} - FCW$ is an expanded notation of *fe*. We note that $f_{RG}(dp(FCW))$ is coarsely set by variations loop, while for acquisition and tracking modes gain coefficients $f'_{RG}(\{da(FCW), dt(FCW)\})$ need to be defined.

Gain coefficient multipliers (see Fig. 3) are the second largest loop area contributors and deserve a wordlength optimization. In our design, gain coefficients are sized so that 1LSB change in frequency command word complies with corresponding bank granularity Δf_{RG} . With the other gain multipliers taken into account

$$\Delta f_{RG_{4,T}} = \left\{ \alpha, \prod_{i=1}^{4} \rho_i \right\} \times \Delta FCW_{1\text{LSB}} \times f_{CKR}, \quad (4)$$

where $\alpha = \frac{1}{4}$ is a damping factor in this ADPLL and $max \{\prod \rho_i\} = 1$ sets no amplitude reduction in the loop filter.

Equation (4) allows to rewrite gain coefficients and find corresponding wordlengths for the greater ratios among desirable reference frequencies

$$\{A,T\} = \left\lceil \log_2\left(f_{RG}'\right) \right\rceil = \left\lceil \log_2\left(\frac{\left\{\frac{1}{4},1\right\} \times f_{CKR}}{\Delta f_{RG_{A,T}}}\right) \right\rceil.$$
 (5)

 Δf_{RG} from the latter equations depends on FCW and two registers regA and regT are provided in this implementation for programming gain estimates.

III. CUSTOM-DESIGNED BLOCKS OF ADPLL

Fig. 4 shows time-to-digital conversion by feeding CKV clock through a line of identical delays and sampling the line at REF rate. Required number of the delays N_{INV} is



Fig. 4. TDC line with power saving and edge alignment circuits.

chosen so that overall delay $N_{INV} \times T_{INV}$ of the chain accommodates the longest DCO output period. T_{INV} was found to be 20 ps after parasitic extraction and for the lowest $F_{CKV} = 1248$ MHz the minimum required N_{INV} is 40. Assuming delay variations in different process corners, 4 additional cells were added. TDC line outputs are sampled with sense-amplifier flip-flops (SAFF), which proved to be fast enough [2] for the target application and feature fully dynamic power consumption.

Measures to reduce power consumption of TDC, running at CKV frequency, are highly desirable. In this design, time period of the TDC line activity is reduced by providing a controlled time window for sampling of the delays' outputs. When bpsn = 1 a narrow time window is opened by edge enabler block after each rising edge of REF frequency. Just after rising edge of REF has arrived, delay line still holds the previous low level of REF signal making en = 1. Delayed and inverted high level of ref REF signal later passes through AND and OR gates resulting in en = 0. Asserting en = 0freezes TDC line in its current state for sampling. Short delay line thus acts to provide enough time for TDC settling after the recent CKV pulse disturbance.

In contrast with our previous implementation [5] delay line is made adjustable to compensate process variations which affect sampling process. The delay tuning is accomplished through controlling driver strength (cs1 < 1:2>) and varactors load (va1 < 1:2> - va4 < 1:2>) of the inverters. According to the



Fig. 5. Micrograph of the MIPI transmitter with ADPLL blocks outlined.

simulations, available delay adjustment is from 0.25 to 2.7 ns.

Edge aligner stabilizes TDC line and consists of a tri-state buffer input and a cross-connected inverter pair with output inverter stage. The output inverters are the same as in TDC line in order to maximize matching in face of process variations. The cross-connected inverters form a latch and retain TDC inputs state during the sampling process.

DCO provides digital-to-frequency conversion and is implemented as a four-stage differential ring oscillator with three distinct tuning schemes. DCO architecture is detailed in [3].

IV. EXPERIMENTAL RESULTS

The ADPLL was fabricated in 40 nm 1P7M CMOS process. The chip micrograph is shown in Fig. 5. The chip area is 1 mm², while ADPLL related circuitry consumes an area of 0.177 mm² ($S_{DCO} = 2860 \ \mu m^2$, $S_{TDC} = 6000 \ \mu m^2$, $S_{EE} = 100 \ \mu m^2$. $S_{Dig} = 168100 \ \mu m^2$ including serial bus logic and auxiliary state machines).

Power consumption of the ADPLL is 2.2 mW at 1.1 V for 1.248 GHz output setting.

Measured phase noise curve is provided in Fig. 6 with $\rho_{1...4}$ set for moderate peaking. To exercise broader input references feature, ADPLL was locked to 10 MHz in this experiment. Obtained phase noise level at 1 MHz offset is -81.4 dBc/Hz.

Fig. 7 shows settling behavior when ADPLL is configured to obtain 1.248 GHz output frequency from mobile standard 26 MHz reference. It takes 17 reference cycles (0.65 μ s) for ADPLL to settle after asserting this configuration.

Measured output spectrum over 1.6 GHz span is plotted in Fig. 8 for the same settings. The far-off spurs are below -45.2 dBc.

V. CONCLUSION

In this paper a clock generator for MIPI M-PHY serial link transmitter with ADPLL core has been presented. ADPLL core was fabricated in 40 nm CMOS featuring speed-enhanced VPA, PVT calibration mode, compact settling monitor and energy saving TDC line which enabled output frequencies generation in 1.2 to 5.8 GHz MIPI M-PHY defined transmission range.



Fig. 6. Measured phase noise when ADPLL settled to 1.248 GHz.



Fig. 7. Measured output frequency when ADPLL settles to 1.248 GHz.



Fig. 8. Measured output spectrum when ADPLL settled to 1.248 GHz.

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