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Efficient surface passivation of black silicon using spatial atomic layer deposition

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Abstract

Nanostructured silicon surface (black silicon, b-Si) has a great potential in photovoltaic applications, but the large surface area requires efficient passivation. It is well known that b-Si can be efficiently passivated using conformal Atomic Layer Deposited (ALD) Al_2O_3, but ALD suffers from a low deposition rate. Spatial ALD (SALD) could be a solution as it provides a high deposition rate combined with conformal coating. Here we compare the passivation of b-Si realized with prototype SALD tool Beneq SCS 1000 and temporal ALD. Additionally, we study the effect of post-annealing conditions on the passivation of SALD coated samples. The experiments show that SALD passivates b-Si surfaces well as charge carrier lifetimes up to 1.25 ms are obtained, which corresponds to a surface recombination velocity $S_{eff,max}$ of 10 cm/s. These were comparable with the results obtained with temporal ALD on the same wafers (0.94 ms, $S_{eff,max}$ 14 cm/s). This study thus demonstrates high-quality passivation of b-Si with industrially viable deposition rates.

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Keywords: spatial atomic layer deposition; nanostructured silicon; high surface area; surface passivation; conformal coating; aluminum oxide;

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1. Introduction

Using black silicon (b-Si) has gained an increasing amount of interest in photovoltaics due to the low reflectance and light trapping properties of the nanostructured silicon surface on a wide spectral range. The large surface area of b-Si leads to a high surface recombination velocity and, therefore, efficient surface passivation is of utmost importance in employing b-Si in photovoltaic devices. Atomic Layer Deposition (ALD) is the method of choice in the deposition of conformal coatings, and using ALD to coat b-Si surfaces with aluminum oxide (Al_2O_3) has already been demonstrated to provide efficient surface passivation [1,2]. ALD-passivated b-Si has been used as a material in record-breaking photovoltaic devices reaching efficiencies above 22 % [3] and in close to ideal photodiodes with high external quantum efficiency over a wide wavelength range [4].

In temporal ALD the coating of high surface area structures such as b-Si can be achieved using long precursor pulses and purge times, or by utilizing a specific reaction chamber in which the precursors can be kept for extended time before purging the chamber with an inert gas [5]. The prolonged residence time facilitates precursor diffusion to the bottom of surface structures, and long purge times are required to also eject the reaction products. Both aforementioned methods are, however, not well suited for high-throughput processing due to their low deposition rate. In addition to residence time, increased precursor concentration and pressure increase the likelihood of precursor infiltration [6].

Spatial ALD (SALD) is a modification of ALD aimed to increase the deposition rate of high-quality conformal coatings and to broaden the reach of ALD [7]. SALD is also well applicable in the coating of porous and High Aspect Ratio (HAR) structures, as demonstrated by Poodt *et al.* [8]. In SALD precursors are usually injected towards the sample surface with a high concentration, which presumably promotes precursor infiltration to the bottom of the structure. So far, few studies on coating porous and HAR structures with SALD have been published, but there is a growing interest in SALD *e.g.* for the coating of porous battery electrodes [9]. In these experiments we study the passivation of planar and nanostructured silicon surfaces using a prototype SALD reactor, Beneq SCS 1000.

2. Experimental

2.1. SALD reactor and ALD processing

Beneq SCS 1000 large-area sheet-to-sheet SALD reactor is presented in Figures 1a and 1b. The reactor consists of a vacuum chamber, a substrate carrier, and a precursor injector system called the coating head. The coating head has 11 precursor zones, which are configured so that metal and oxidising precursors alternate. The substrate plate is moved back and forth underneath the coating head so that the substrate is alternatingly exposed to both precursors, and the thickness of the deposited film can be controlled by adjusting the number of passes under the coating head. The maximum effective coating area is 400 mm x 500 mm. There is approximately a 1 mm gap between the coating head and the substrate plate. Process pressure can be adjusted from 50 mbar up to near-atmospheric pressure, and substrate translation speed can be varied between 0.3 and 30 m/min.

In SALD passivation trimethylaluminum (TMA) and H_2O were used as precursors at 150°C. The studied line speeds were 1.5, 4.5 and 9 m/min. Growth per cycle (GPC) ranged from 1.27 Å/c with 9 m/min to 1.49 Å/c with 1.5 m/min, which suggests that with higher line speeds fully saturating surface reactions were not achieved. With the highest line speed a deposition rate of 2.9 nm/min was reached. SALD was compared to thermal temporal ALD passivation, realized with a Beneq TFS 500 ALD tool using TMA and H_2O as precursors at process temperature of 200°C [1]. Samples were passivated with approximately 20 nm thick Al_2O_3 layers on both sides of the samples with both methods. With SALD the passivation layer was first deposited on one side of the wafer, after which the wafer was turned upside to repeat the passivation process on the other side of the sample.

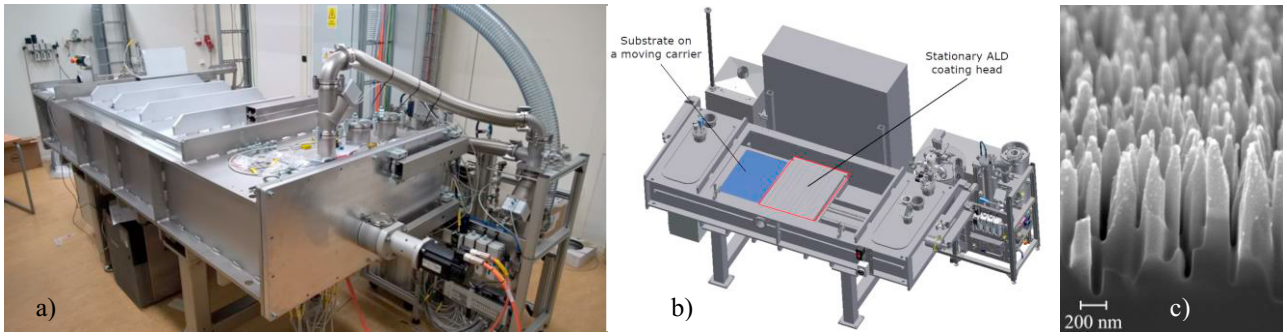

Fig. 1. (a) A photograph and (b) a schematic of the Beneq SCS 1000 sheet-to-sheet SALD reactor installed at the Beneq facilities in Espoo, Finland. (c) An SEM micrograph of a freshly etched b-Si surface.

2.2. Materials and characterization

Float Zone wafers (~1 Ωcm, 4 inch, 250 µm, p-type) were used as substrates. b-Si surface was prepared on some of the wafers on both sides using cryogenic deep reactive ion etching *i.e.* ICP-RIE using process parameters reported in [1], and remaining samples were left unetched to be used as planar reference wafers. A scanning electron microscope (SEM) image of typical b-Si surface is presented in Figure 1c. SALD passivated wafers were post-annealed at temperatures ranging from 370 to 450°C in N_2 and H_2/N_2 atmospheres to study the effect of the annealing conditions to charge carrier lifetime τ, total film charge Q_{tot} and interface defect density D_{it}. In previous experiments annealing at 425°C for 30 minutes in a N_2 atmosphere yielded good lifetimes for samples passivated with the employed temporal ALD process [10], so these annealing conditions were chosen also for the reference samples in this study. Table 1 summarizes all utilized process and annealing parameters. τ was characterized using photoconductance method in the transient mode (WTC-120 Sinton Instruments) and the corresponding maximum surface recombination velocities $S_{eff,max}$ were calculated from them assuming infinite bulk lifetime. Passivation layer Q_{tot} and D_{it} were measured using contactless CV (COCOS) [11] with a Semilab PV-2000A instrument.

Table 1. Studied process parameters for SALD and temporal ALD passivation of both planar and b-Si samples.

Passivation method	Process temperature (°C)	Line speed (m/min)	Annealing temperature (°C)	Annealing atmosphere
SALD	150	1.5	370	H_2/N_2
		1.5	400	N_2
		1.5	400	H_2/N_2
		1.5	450	N_2
		4.5	370	H_2/N_2
		9	370	H_2/N_2
Temporal ALD	200	-	425	N_2

3. Results and discussion

3.1. Annealing conditions

First, suitable parameters for post-deposition annealing were determined. Both planar and b-Si substrates were passivated with the lowest line speed of 1.5 m/min, and all such samples were annealed for 30 min in the following conditions: H_2/N_2 at 370°C, N_2 at 400°C, H_2/N_2 at 400°C, and N_2 at 450°C. Lifetime results of both planar and b-Si samples are presented in Figures 2a and 2b. The figures show that annealing in H_2/N_2 at 370°C yields the highest charge carrier lifetime for both planar and nanostructured samples. As a comparison, the planar substrate annealed at

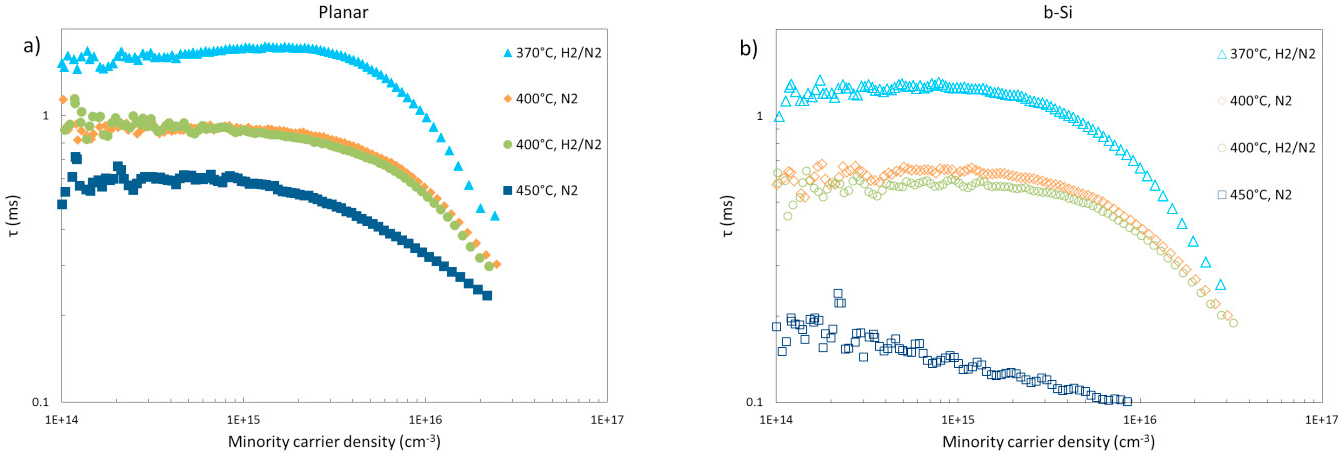

Fig. 2. τ of planar (a) and b-Si (b) samples passivated with a line speed of 1.5 m/min and annealed in varying conditions.

370°C, reached 1.7 ms at an excess carrier density of 10^{15} cm^{-3} with the corresponding $S_{eff,max}$ of approximately 7 cm/s. For b-Si annealed at the same conditions τ was 1.25 ms and $S_{eff,max}$ 10 cm/s.

As there were notable differences in the lifetime depending on the annealing conditions, it was expected to observe differences in Q_{tot} and D_{it} as well. Both Q_{tot} and D_{it} were measured for planar samples, but only Q_{tot} of b-Si samples could be accurately determined as in previous studies [2]. Q_{tot} of the planar samples were in the same order of magnitude with all annealing conditions, it only varied from $-3.3 \cdot 10^{12}$ cm^{-2} to $-4.5 \cdot 10^{12}$ cm^{-2}. Also D_{it} of the planar substrates annealed with different conditions were comparable with each other, in the order of $3.0 \cdot 10^{11}$ $cm^{-2}eV^{-1}$. The measured film charge in b-Si samples was higher with all annealing conditions than in the planar samples, which can be attributed to the fact that the measured charge value is effective and surface area dependent as shown before [10]. The best passivation for both sample types was achieved by annealing in H_2/N_2 at 370°C, which yielded the lowest charge on both planar and b-Si substrates. Therefore, the quality of field-effect passivation does not explain the differences in the charge carrier lifetimes. The trend of charge carrier lifetimes can neither be attributed to enhanced chemical passivation, as D_{it} was in the same order with all annealing conditions.

3.2. Increased line speed

The industrial feasibility of surface passivation processing with the utilized SALD tool was inspected by coating planar and b-Si substrates with higher line speeds (4.5 and 9 m/min). These samples were annealed in H_2/N_2 at 370°C, which yielded the highest lifetimes for both planar and b-Si substrates as shown above. Comparison of τ for the samples passivated with different line speeds is presented in Figure 3a, and the corresponding Q_{tot} and D_{it} values are presented in Figure 3b.

The highest lifetime for b-Si samples was obtained with the slowest line speed, 1.5 m/min (1.25 ms at an excess carrier density of 10^{15} cm^{-3}), but also faster line speeds yielded efficient passivation with lifetimes in the same order of magnitude. As the highest lifetime was obtained with the slowest line speed, it is possible that the longer precursor exposure time provides a more uniform passivation layer than with higher line speeds. For planar samples the charge carrier lifetimes followed a different trend than b-Si samples. The highest lifetime in the planar substrates was obtained with 9 m/min, which yielded $\tau = 3.44$ ms with $S_{eff,max} = 4$ cm/s. The fact that the highest lifetime for planar substrates was obtained with the fastest line speed might indicate that with slower line speeds the H_2O surface reactions potentially oversaturated, which yielded a high OH-group concentration in the film. The residual hydrogen might evaporate during the annealing, which in turn could cause minor blistering of the passivation layer. However, more accurate analysis is required to confirm the viability of this hypothesis.

Q_{tot} and D_{it} of the films deposited on planar substrates were similar with all line speeds. Total film charge in the b-Si samples was, again, higher than in planar substrates, and there were only small differences between Q_{tot} in b-Si

substrates in terms of line speed. As only small differences were generally observed in film charge and defect density in relation to line speed, further analysis on film composition and possible delamination is required to verify the exact passivation mechanisms in this case.

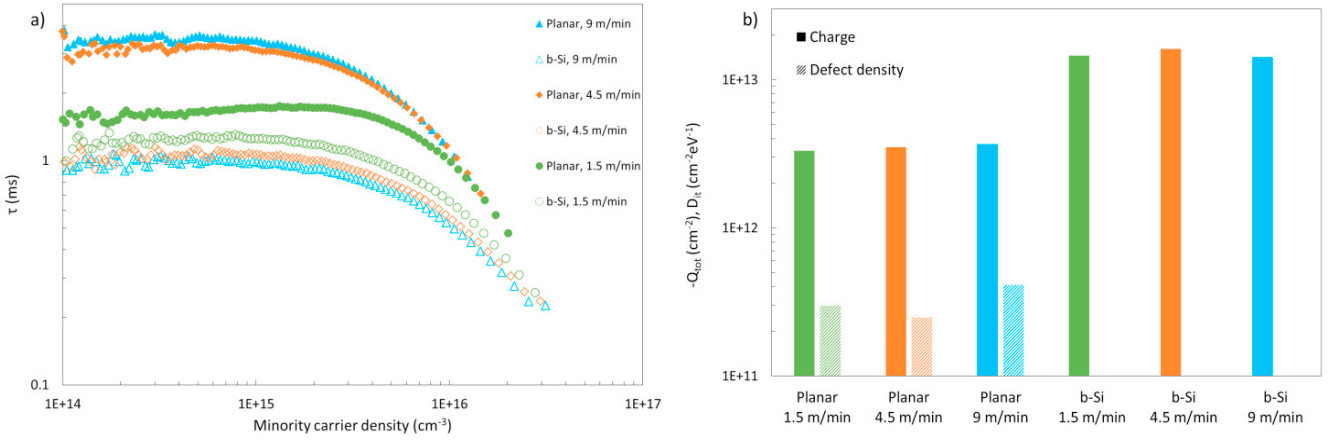

Fig. 3. (a) τ and (b) Q_{tot} and D_{it} of planar and b-Si samples coated with SALD with different line speeds. Samples were annealed in a H_2/N_2 atmosphere at 370°C.

3.3. Comparison of spatial and temporal ALD

Processing with the prototype SALD tool was confirmed to be a viable technique for the surface passivation of both planar and b-Si surfaces, and annealing in a H_2/N_2 atmosphere at 370°C yielded the best lifetime results for both sample types. The highest charge carrier lifetimes of SALD coated planar and b-Si wafers were compared with the results obtained with temporal ALD. τ as a function of minority carrier density of SALD and temporal ALD passivated wafers are presented in Figure 4a, and Q_{tot} and D_{it} are presented in Figure 4b. As seen in the figure, spatial ALD passivation yields slightly higher τ in both planar and b-Si wafers than temporal ALD passivation.

In the SALD passivated b-Si Q_{tot} was $-1.45 \cdot 10^{13}$ cm^{-2}, which was in the same order as with temporal ALD. With temporal ALD D_{it} for planar substrates was $1.8 \cdot 10^{12}$ $cm^{-2}eV^{-1}$, while with SALD D_{it} was over double this value. The annealing conditions of temporal ALD passivation need to be studied further. However, the conditions which yield the highest lifetime can be different for SALD and temporal ALD passivated samples despite the same ALD precursors, as deposition temperature can have a significant effect on the chemical composition of the deposited Al_2O_3 films [12]. Further experiments with other SALD processes, such as using ozone as on oxidant, could provide further insight into the passivation mechanisms.

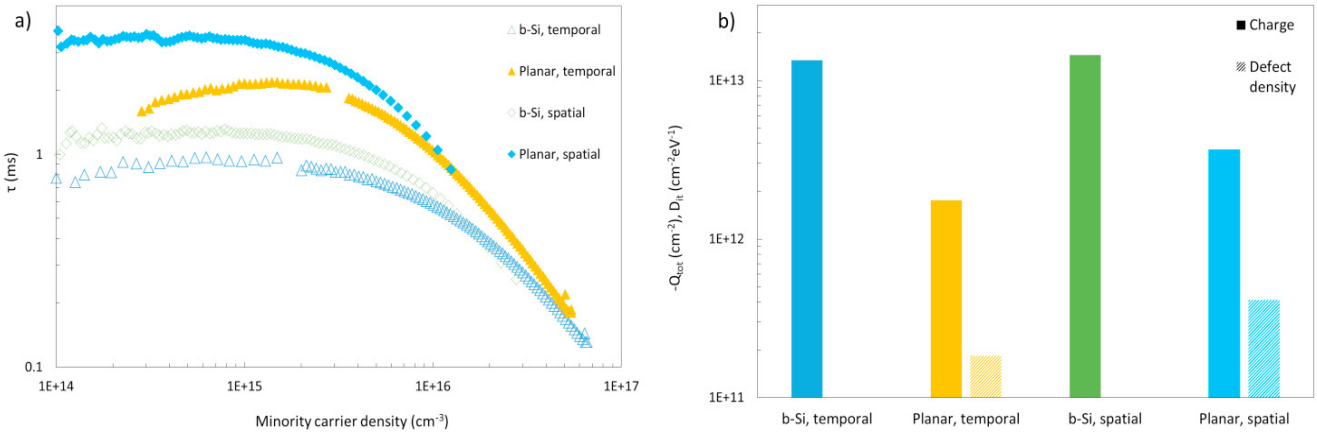

Fig. 4. (a) τ and (b) Q_{tot} and D_{it} of planar and b-Si samples coated with SALD and temporal ALD.

4. Conclusions

In this study we have shown that SALD can provide efficient surface passivation in planar silicon and b-Si. These results indicate that the conformal coating of high surface area structures such as b-Si is indeed feasible with SALD. Total film charges were in the same order with all annealing conditions and line speeds, but there were significant differences in the obtained lifetimes. Thus, further experiments are required to gain further understanding on the passivation mechanisms, as chemical passivation and field effect passivation alone do not explain the observed lifetime behavior. However, efficient passivation of both planar and b-Si substrates was achieved with all line speeds, even with 9 m/min, which demonstrates excellent process scalability and suitability for industrial-scale applications.

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