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Achieving low-temperature wafer level bonding with Cu-Sn-In ternary at 150 °C

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ABSTRACT

In this work, a low-temperature wafer-level bonding process at 150 °C was carried out on Si wafers containing 10 µm-sized microbumps based on the Cu-Sn-In ternary system. Thermodynamic study shows that addition of In enables low-melting temperature metals to reach liquid phase below In melting point (157 °C) and promotes rapid solidification of the intermetallic layer, which are beneficial for achieving low-temperature bonding. Microstructural observation shows high bonding quality with low amount of defect. SEM and TEM characterization concludes that a single-phase intermetallic formed in the bond and identified as Cu6(Sn,In)3 with a hexagonal lattice. Mechanical tensile test indicates that the bond has a mechanical tensile strength of 30 MPa, which are adequate for 3D heterogeneous integration.

The motivation to keep up with Moore’s prediction has set heterogeneous integration as one of the milestones in semiconductor industry. Stacking wafers containing high-density verticals vias, such as TSV, with micropumps is amongst the key component in achieving 3D heterogeneous integration [1–3]. Wafer-level bonding, in particular, received special attention to enable low cost-yet high throughput fabrication [4].

Amongst various wafer-level bonding techniques, the solid-liquid interdiffusion (SLID) bonding process has several traits that make it attractive. It utilizes low-to-moderate bonding temperatures to form intermetallic compound (IMC) with a much higher re-melting temperature from low-melting temperature metal and high-melting temperature substrate [3,5]. The conductive nature of the bonds also favours it as a vertical interconnect between the substrates, which can be used for heterogeneous integration when integrated with TSV [6].

However, some challenges remain in the SLID bonding process. Typical SLID bonding processes using Cu-Sn system are conducted above the Sn melting point at 280–320 °C [3,7]. This temperature is often not low enough for temperature-sensitive components, such as micro-bolometers or low-curie temperature poled piezoelectric [7,8]. Furthermore, local and global residual stress induced during the cooling down process remains relatively high, which makes the application difficult for bonding heterogeneous materials with a high coefficient of thermal expansion (CTE) mismatch [8–10]. Other system, such as Cu-In, utilize a much lower melting temperature of In are typically conducted between 170 and 200 °C. Nevertheless, it comes with the disadvantage of longer bonding times or poor thermodynamic stability from the metastable phase, such as Cu5In transformation to Cu4In3 at 310 °C accompanied by void formation [3,11].

Recent study re-explores SLID bonding processes based on the Cu-Sn-In ternary system to reduce both bonding temperature and time using In stabilizing effect on the liquid phase, supported by optimized design of metallization layer thickness [12]. Fig. 1(a) illustrates the vertical section (48Sn,52In)-Cu from the ternary Cu-In-Sn phase diagram superimposed with the binary Cu-Sn and Cu-In phase diagrams. The diagram shows that through Sn-In eutectic behaviour the melting point of lower temperature metal is significantly reduced under the In melting temperature of 157 °C, which indicates that the bonding process could be done at a much lower temperature than the Cu-Sn or Cu-In system [13]. The diagram also highlights that at 250 °C Cu solubility doubles in the Sn-In liquid phase compared to only Sn liquid phase, which indicates a faster intermetallic solidification, and therefore faster bonding process [12].

A finite element study was conducted to study the local residual stress effect as a result of bonding temperature reduction. Fig. 1(b) illustrates the COMSOL model used to study the local residual stress profile of a 10 µm square bump consisting of Cu-Cu6Sn5-Cu layers. The
copper and intermetallic layer thickness were set to 2.5 µm and 5.5 µm, respectively. Cu₆Sn₅ was selected as the intermetallic layer in the model as it is the only phase that would be formed below 200 °C and is expected to have similar thermo-mechanical properties to the predicted Cu₆(Sn,In)₅. The Young’s modulus and Poisson’s ratio used in the model were obtained from the reference [14], while other material properties were taken from COMSOL library. The simulated von Mises Stress profile acting on the microbump diagonal cross-section (marked in Fig. 1(b)), which depicts the residual stresses, is presented in Fig. 1(c). Based on the figures, reducing the bonding temperature from 250 to 150 °C reduces the stresses on the intermetallic layer by roughly 30%, which signifies the importance of achieving low-temperature SLID bonding to improve the bond’s reliability.

In this work, Cu-Sn-In based SLID bonding process was applied to bond 4-inch Si wafers. A detailed description of the fabrication process flow can be found in the Ref. [9]. The wafers consisting the microbumps with a total bonding area of 252 mm² were brought together with a contact force of 7.5 kN bonded under vacuum conditions at 150 °C for 1 h. Fig. 2(a) shows the SEM cross-sectional images on the 10 µm bumps after the bonding process, which indicates that the bonds were successful. Higher magnification image in Fig. 2(b) shows that not all copper had reacted during the bonding process. Furthermore, Sn-In squeeze-out could be observed at the edge of the bond indicating that the metals follow the eutectic behaviour of the alloy to form a liquid phase at a lower melting temperature compared to pure In (157 °C). EDS observation conducted at the points marked 1–3 gives an average elemental composition of Cu, Sn, and In as 55.5 ± 1.5 at.%, 29.1 ± 1.1 at.%, and 15.4 ± 0.4 at.%, respectively. This result is close to the reported elemental composition of Cu₆Sn₅, with In substituting Sn in the intermetallic sublattice [12,15,16].

Chip level mechanical pull test exhibited that the bond has a mechanical tensile strength of 32.7 ± 4 Mpa. The fracture surfaces after the testing were observed in SEM and are shown in Fig. 2(c) and (d). The SEM micrograph in Fig. 2(c) shows that all bonds have a similar fracture surface in the intermetallic layer indicating that the bonds are forming homogeneously across the chips. EDS analysis taken at point 4–6 shows the Cu, Sn, In elemental composition as 59.5 ± 0.8 at.%, 25.1 ± 0.7 at. %, and 15.4 ± 0.4 at.% respectively. These results also show close value
to the reported phase of Cu₆Sn₅₆, despite the slightly higher Cu concentration on the fracture surface EDS due to electron beam penetration into the Cu layer.

Further observation was conducted with a FIB cut on the microbump cross-section. Higher magnification image in Fig. 3(c) clarifies that the bond has a hairline defect across the centre, which could be a non-bonded surface that initiates the failure in the mechanical pull-test, as observed on the microbump topside in Fig. 2(d). EDS mapping on the microbump cross-section indicates that the In and Sn distributed evenly across the bond without any segregation, indicating the intermetallic consisted of a single-phase Cu₆(Sn,In)₅₂. Furthermore, the SEM results also indicate that the ζ phase (Cu₃(Sn,In)) does not form in the interface, which is usually associated with microvoid formation at Cu to intermetallic interfaces [7,12]. The simple reason for this is the lack of driving force for the formation of this phase, which typically forms above 200 °C [15,17].

A lamella formed from the microbump was used for a more detailed observation using the TEM. Fig. 4(a) and (b) show a clear microstructure of the bond, that confirms a successful bond without any interfacial voids and high crystallinity. The enlarged section on the intermetallics in Fig. 4(c) shows that it consists of grains roughly larger than 200 nm, while at the interface region with Cu the grains have a much finer grain size, as presented in Fig. 4(d). The two-layered structure, namely the duplex structure, has been reported to be caused by the difference in the interdiffusion rate of Cu and Sn-In. Faster Cu diffusion rate into the Sn-In liquid phase during the solidification process resulted in a large-sized grain. On the other hand, Sn-In diffusion through the Cu liquid phase during the solidification process resulted in a large-sized interdiffusion rate of Cu and Sn-In. Faster Cu diffusion rate into the Sn-In duplex structure, has been reported to be caused by the difference in the η-Cu₆(Sn,In)₅₂ phase (Cu₃(Sn,In)) does not form in the interface, which is usually associated with microvoid formation at Cu to intermetallic interfaces [7,12]. The simple reason for this is the lack of driving force for the formation of this phase, which typically forms above 200 °C [15,17].

The EDS mapping confirms that the intermetallic layer consisted of Cu, Sn and In elements that are distributed homogeneously, agreeing with previous observation that the bond consisted of a single phase. The shadowing effect during the lamella polishing process causes a higher In concentration at Cu/Cu₆(Sn,In)₅₂ interface and does not imply another phase exists in the finer grain structure. The Sn-In homogenous distribution is ensured by the homogenous mixing of Sn and In layers, as the metal layers were deposited on both substrates with equal thickness. Fig. 4(f) shows the selective area electron diffraction (SAED) patterns obtained from three different zone axis at the grain marked in Fig. 4(c). The diffraction patterns on each zone axis at each respective tilt position correspond with the known hexagonal structured ζ-Cu₆Sn₅ in the P6₃/mmc space group [18]. Thus, it can be concluded that the intermetallic was composed of a single phase η-Cu₆(Sn,In)₅₂.

To conclude, wafer-level bonding has been successfully demonstrated with 10 μm sized square bump at 150 °C based on the Cu-Sn-In ternary system. Cross-section observations on the microbump show some squeeze-out formation, which agrees with the thermodynamic study that the addition of In reduces the temperature to form a liquid phase. SEM and TEM microstructure observations conclude that the bonds have a high crystallinity belonging to the single phase of η-Cu₆(Sn,In)₅₂ with hexagonal lattice. Large grain observation in the duplex layer structure indicates that a rapid dissolution of Cu into the Sn-In melt occurs, and the small grain indicates a slower Sn-In diffusion into the Cu substrate. The results from this study highlight the possibility of low-temperature wafer-level bonding and give the motivation to investigate its reliability.

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Declaration of Competing Interest

The authors declare no conflict of interest in the submission of this manuscript.

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