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A Compact Untrimmed 48ppm/°C All MOS Current Reference Circuit

***Abstract*—An ultra-low power and low-cost (area efficient) nano-ampere current reference circuit designed in a 65 nm technology is presented in this paper. The proposed circuit is a resistorless beta multiplier current reference circuit that uses self cascode composite MOSFETs in triode region. Circuit analysis has been discussed in the paper. The simulated circuit consumes power of 550 nW at a nominal operating voltage of 1.33 V and occupies area of 0.0031 mm^2. The design provides a line regulation of 1.9%/V over an operating voltage range of 1.25 V to 1.4 V. Temperature coefficient (TC) of the circuit at nominal voltage of 1.33 V is 48 ppm/°C for a wide temperature range of -40 °C to 85 °C. Output current of the circuit at nominal voltage is 104.2 nA with a small process variation of only 4%.**

***Index Terms*—Current reference, low-power, low temperature coefficient, self-cascode transistor, CMOS beta multiplier.**

I. Introduction

A reference current generator is basic building block of analog circuits such as analog-digital converters, oscillators, amplifiers, etc. The increasing demand for ultra low power designs for applications such as internet of things, wireless sensor nodes, etc. makes the need for a low cost, small area and low power consumption reference current circuit, essential. Current generated needs to be free of any process, supply voltage and temperature (PVT) variation.

A classical beta multiplier reference generator uses a resistor for current generation but the area overhead is large, resistivity of an on-chip resistor may vary with technology and thermal variation of output current is significantly high. To solve these issues associated with on-chip resistors, a resistor-less beta multiplier was developed by using a MOSFET operating in triode region [2], however the temperature dependency of this circuit is not well defined. Several variations of resistorless current generation circuits have been reported in [3], [4], [6], [9] and [10] where the research focuses on thermal stability [3] - [7], process variation [7], [10], and power consumption. In [3], output current is generated by biasing transistor near its zero temperature coefficient point. The circuit demonstrates a low power consumption and TC of 127 ppm/°C but ratio of supply to output generated current is high. [4] uses a curvature compensation scheme to generate a very low TC, but area overhead is quite large. [8] uses two triode MOSFETs in parallel active as a positive and negative TC resistor, the circuit generates 500 nA of current and has a TC of 119 ppm/°C but needs a trimming circuit for tuning of TC. In [7] a curvature and process compensated circuit is designed by using curvature compensation method, the circuit shows a low TC and is PVT compensated at the expense of complex circuitry with an additional trimming circuit and increased area. [9] has a very low TC but the circuit uses larger MOSFETs and additional complex compensation sub-circuits. Therefore, in consideration of this background, a trade-off is made in either compensating temperature and/or process variation, lowering power or reducing the area.

A compact temperature compensated resistorless beta multiplier current reference circuit is presented in this paper. The fact that threshold voltage of MOS transistors are complementary to absolute temperature is exploited in this design. Combining this with [2] results in a temperature compensated reference circuit specialized for ultra-low power applications. The circuit is thermally compensated and consumes small area. Performance of the proposed reference circuit is comparable to state of the art designs [3]- [9].

This paper is organized as follows: Section II discusses the designed circuit and a circuit analysis is done further to understand the working principle of design. Section III presents postlayout simulation based results and section IV draws final conclusions.

II. Proposed Circuit

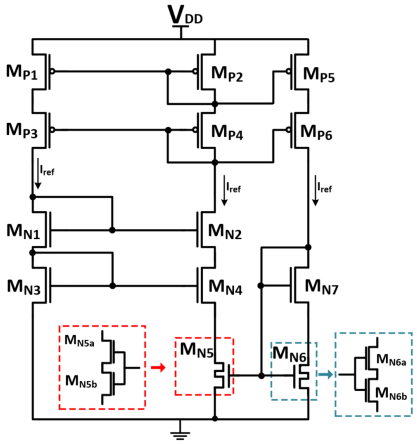

Fig. 1. Schematic of the proposed current reference with self-cascode composite MOSFETs and their equivalent circuit

A. Circuit Description

The reference circuit proposed is a modification of resistorless beta multiplier current reference circuit in [2]. Implemented current reference circuit is shown in Figure 1, the startup circuit is not shown in this schematic. MOSFETs M_{P3}, M_{P4}, and M_{N7} are operating in saturation region, M_{N3}, M_{N4} are operating in subthreshold region and M_{N5}, M_{N6}, are operating

in linear region. The bias voltage required for the MOSFETs to operate in linear region is generated from MOSFET M_{N7}. I_{ref} is the bias current generated by the circuit. Each branch in the circuit should have high impedance in order to improve line sensitivity. The circuit therefore uses cascode current sources consisting of M_{P1} and M_{P3}, M_{P2} and M_{P4}, M_{N1} and M_{N3}, M_{N2} and M_{N4}, thus providing required impedance. M_{N5} and M_{N6} are used in self-cascode structure, thereby providing a much larger effective channel length than the single equivalent MOSFET [12]. Moreover, the two self-cascode NMOS M_{N5a} and M_{N5b} in Figure 1 are on the same substrate therefore they are shown as a single equivalent MOSFET symbol in the circuit proposed in [11], same is done for M_{N6}.

B. Proposed Design Analysis

Applying KVL in loop formed by M_{N7}, M_{N6} and M_{N5},

$$V_{GS5} = V_{DS6} + V_{GS7} \tag{1}$$

where V_{GS5} is the gate-source voltages of NMOS M_{N5}, V_{DS6} is the drain-source voltage of NMOS M_{N6} and V_{GS7} is the gate-source voltage of NMOS M_{N7}. Since NMOS M_{N7} is operating in saturation region, therefore,

$$V_{GS7} = V_{TH7} + \sqrt{\frac{2I_{ref}}{K_n S_7}} \tag{2}$$

Where K_n is the transconductance parameter, V_{TH} is the threshold voltage, and S_7 is the aspect ratio of M_{N7}. Gates of M_{N5} and M_{N6} are connected together and source of both transistors are connected to ground hence,

$$V_{GS6} = V_{GS5} = V_G \tag{3}$$

M_{N5} and M_{N6} are operating in linear region and the current flowing through them is,

$$\begin{aligned} I_{ref} &= K_n S_6 (V_G - V_{TH6}) V_{DS6} \\ &= K_n S_5 (V_G - V_{TH5}) V_{DS5} \end{aligned} \tag{4}$$

Substituting (2), (3), and (4) to equation (1), and solving the quadratic equation obtained for V_G,

$$V_G = \frac{1}{2}\left(\sqrt{\frac{2I_{ref}}{K_n S_7}} + V_{TH7} + V_{TH6}\right) \tag{5}$$

Further solving for V_{DS6} from equations (1), (2), (4) and using V_G obtained in (5) will result in

$$V_{DS5} = \frac{S_6\left(\sqrt{\frac{2I_{ref}}{K_n S_7}} + V_{TH7} - V_{TH6}\right)^2}{2S_5\left(2V_{TH5} - \sqrt{\frac{2I_{ref}}{K_n S_7}} - V_{TH7} - V_{TH6}\right)} \tag{6}$$

By applying KVL in circuit formed by M_{N3}, M_{N4} and M_{N5},

$$V_{GS3} = V_{GS4} + V_{DS5} \tag{7}$$

Drain current (I) of MOSFET in subthreshold region is given by,

$$I = I_{D0} S e^{\frac{V_{GS} - V_{TH}}{\eta \frac{kT}{q}}} \tag{8}$$

where S is the aspect ratio, η is the subthreshold slope factor, k is the Boltzmann constant, q is electronic charge, T is temperature and I_{D0} is the current that flows when V_{GS}=V_{TH}. Since M_{N3} and M_{N4} are in subthreshold, therefore, V_{DS5} can be calculated from (7) and (8) as

$$V_{DS5} = \frac{\eta kT}{q} ln\left(\frac{S_4}{S_3}\right) \tag{9}$$

Where S_3 and S_4 are aspect ratios of NMOS M_{N3} and M_{N4}. The carrier mobility μ_n and thermal voltage (kT/q or V_T) are temperature dependant and can be expressed by

$$\mu_n = \mu_0 (T/T_0)^{-K_{\mu n}} \tag{10}$$

$$V_T = \frac{kT}{q} = V_{T0}\left(\frac{T}{T_0}\right) \tag{11}$$

Here T_0 is the room temperature, V_{T0} is the thermal voltage at T_0 and $K_{\mu_n}$is the temperature coefficient of μ_n. K_{μ_n} is process dependent and is generally between 1.5-2. The threshold voltage variation with temperature according to [13] can be written as

$$V_{TH} = V_{TH0} - \alpha(T - T_0) \tag{12}$$

V_{TH0} is the threshold voltage at temperature T_0, α is the temperature coefficient of threshold voltage. As α is positive, therefore, according to equation (12) increasing temperature will decrease the threshold voltage. Combining equation (6), (9), (10) and (11) , I_{ref} is obtained as follows,

$$\begin{aligned} I_{ref} = \Bigg(& \frac{1}{2}\mu_0(T_0)\left(\frac{T}{T_0}\right)^{2-K_{\mu n}} \frac{K_n S_7}{2S_6^2} \Bigg) \cdot \\ & \underbrace{\left[2S_5\left(\frac{\eta k}{q} ln\left(\frac{S_4}{S_3}\right)(T/T_0)\right)\right]^2}_{\text{PTAT}} \\ & + \underbrace{S_6^2 (V_{TH6} - V_{TH7})^2}_{\text{CTAT}} + \\ & \underbrace{2S_5 S_6\left(\frac{\eta kT}{qT_0} ln\left(\frac{S_4}{S_3}\right)(2V_{TH5} + V_{TH7} - 3V_{TH6})\right)}_{\text{CTAT}}] \end{aligned} \tag{13}$$

From equation (13), terms affecting the temperature dependence of the current are threshold voltages of MOSFETs M_{N5}, M_{N6} and M_{N7}, the carrier mobility and thermal voltage. Equation (13) also shows the relationship between I_{ref} and the aspect ratio of NMOS M_{N3} to M_{N7}, which can be modified in order to achieve a desired output current. Furthermore, differentiating equation (13) w.r.t. temperature (T), such that the TC (dI_{ref}/dT)=0 i.e. minimum temperature coefficient, the result obtained is dependant on the thermal slopes of threshold voltages of M_{N5} to M_{N7}. Since threshold voltage is complementary to temperature (CTAT), hence aspect ratios can be modified to change the CTAT behaviour of the circuit. Carrier mobility and thermal voltage provide the proportional

to temperature dependence (PTAT). Therefore, by choosing the aspect ratios which cancels the mobility temperature dependence with threshold voltage dependence, a thermally compensated circuit is obtained.

III. Simulation Results

The proposed circuit is designed in a 65 nm CMOS technology and occupies an area of 0.0031 mm^2. The layout of the circuit is shown in Figure 2. Postlayout simulations of

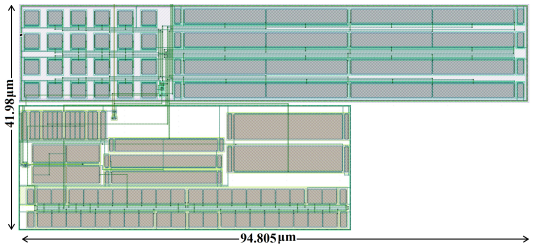

Fig. 2. Layout of the proposed circuit with dimensions

this circuit were performed to validate the functionality of the design. Current generated by the circuit is plotted for different supply voltages over a wide range of temperature from -40 °C to 85 °C. Nominal operation voltage of this circuit is 1.33 V where a bias current of 104.2 nA is achieved.

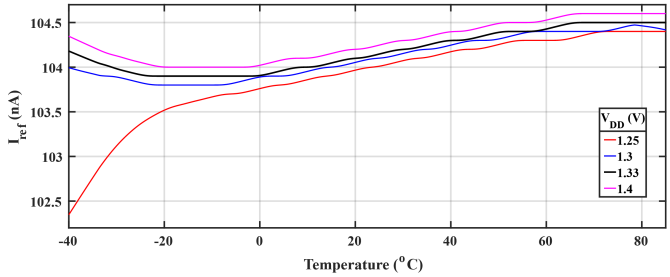

Fig. 3. Temperature characteristics of generated output current with variation of supply voltage

Figure 3 shows the output current I_{ref} over the forementioned temperature range. As evident from this simulation result, the circuit shows little variation w.r.t. temperature for the nominal operating voltage of 1.33 V. The TCs of this circuit at operating voltages of 1.25 V, 1.3 V, 1.33 V and 1.4 V are 160 ppm/°C, 49.53 ppm/°C, 48 ppm/°C and 46.7 ppm/°C, respectively. A minimum TC of 46.7 ppm/°C is obtained when the supply voltage is 1.4 V as shown in Figure 4. The TC after supply voltage of 1.285 V becomes almost constant w.r.t. increase of supply voltage attaining a value of approximately 47 ppm/°C. All MOSFETs reach their desired operating region at an minimum voltage of 1.15 V. Figure 4 also shows output current plot with the supply voltage varying from 1.15 V to 1.4 V, the circuit shows a line sensitivity (LS) of 1.9 %/V for the operating voltage range of 1.25 V to 1.4 V. The circuit consumes an average power of 0.55 μW at 1.33 V supply voltage, generating I_{ref}= 104.2 nA.

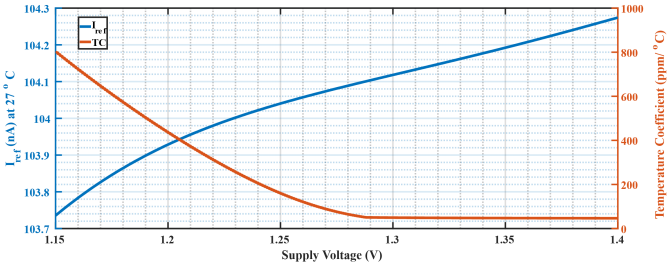

Fig. 4. Supply dependence of temperature coefficient and line sensitivity

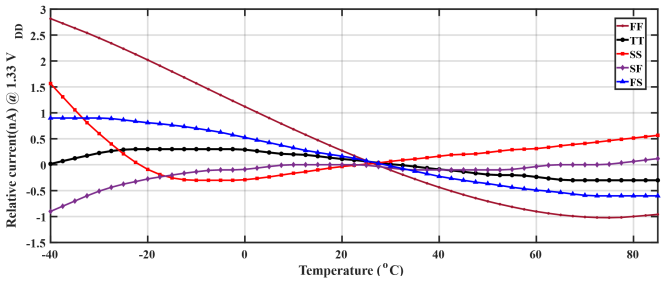

Fig. 5. Relative generated current (w.r.t. room temperature) with process and temperature variations

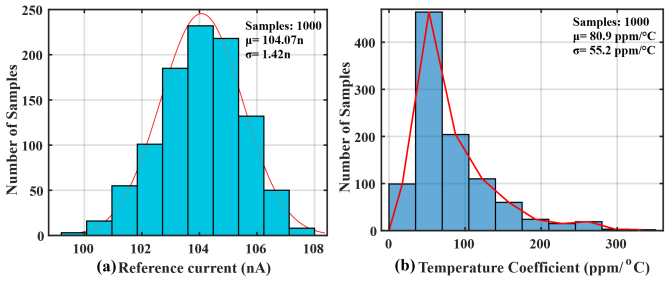

Fig. 6. Simulated distribution of (a) Output current (b) TC

The sensitivity of the circuit w.r.t. process corners is shown in Figure 5, here the plot has been normalized for room temperature (27°C) in order to account for changes in current across temperature range. In order to evaluate the robustness of the circuit Monte Carlo (MC) process variation simulations are performed (Figure 6(a) and 6(b)) for 1000 samples at a supply voltage of 1.33 V. The mean (μ) output current of the simulated distribution is 104.07 nA with a deviation (σ) of 1.42 nA, therefore the process variation ($3\sigma/\mu$) of this circuit is 4%. MC process variation of TC shows μ= 80.9 ppm/°C and σ = 55.2 ppm/°C with more than 74% of samples having a TC of less than 100 ppm/°C. Output noise simulations under process corner in Figure 7 shows the circuit generates a low noise of 12.5 $\mu/\sqrt{Hz}$ at 1 Hz for TT corner which is much lower than the state of the art [7]. In the same Figure, PSRR performance with frequency is shown which depicts the PSRR at 1 Hz is -64.19 dB and remains -63.83 dB at 100 Hz.

Table I summarizes the performance of the circuit obtained in simulations. A comparison with state of the art work has been made in this table. A modified figure of merit (FOM)

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH RELATED STATE OF THE ART

	This Work	ISCAS [7]	ISCAS [4]	ISCAS [3]	PRIME [5]	TCAS-II [1]	ISCAS [6]
Year of Publication	**2022**	2020	2019	2017	2017	2017	2010
Technology(µm)	**0.065**	0.18	0.18	0.18	0.18	0.35	0.18
Supply Voltage (V)	**1.25-1.4**	1.38-3	1.2-2	0.9-1.8	1.7-1.8	1.9-3.6	2
Average Iref (nA)	**104.2**	66	142.5	10.95	1000	16000	10000
TC (ppm/°C)	**48**	67.04	40	127	29.6	105	170
Temperature range (°C)	**-40- 85**	-50- 100	-40- 85	-20- 120	-40- 140	0- 110	-20- 120
Line Sensitivity (%/V)	**1.9**	1.413	1.45	0.86	-	4	3
Process Variation ($3\sigma/\mu$ %)	**4**	12	9.4	11.5	9.1	10.2	12.7
Power Consumption(µW)	**0.55**	0.275	1.231	0.122	90	60.8	80
Area (mm^2)	**0.0031**	0.098	0.02	0.018	0.05	0.065	-
Circuit-All MOS	**Yes**	No	Yes	Yes	No	No	No
FOM (%ppm/°C^2V)	**0.116**	0.228	0.209	0.554	-	0.775	1.847
Measurement type	**Simulation**	Simulation	Simulation	Simulation	Simulation	Measurement	Simulation

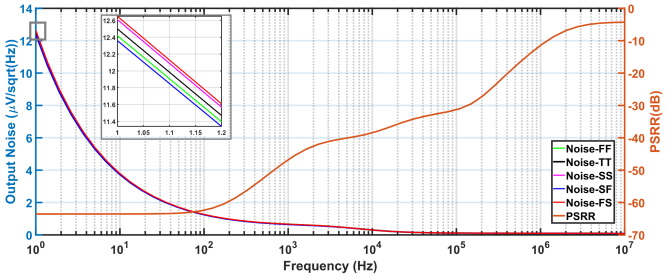

Fig. 7. Output noise of the circuit across all process corners and PSRR at supply voltage of 1.33V

based on [4] is used which denotes the relationship between TC (ppm/°C), total input current (I_{Total}, nA), reference output current (I_{ref}, nA), temperature range (TR, °C), line sensitivity (LS, %/V) and process variation ($3\sigma/\mu$). The proposed FOM takes into account power consumption, the process ($3\sigma/\mu$), voltage (LS) and temperature variations(TC) and is given by:

$$FOM\left(\frac{\%ppm}{^{\circ}C^2V}\right) = \frac{TC}{TR}.\frac{I_{Total}}{I_{ref}}.LS.\frac{3\sigma}{\mu} \qquad (14)$$

IV. CONCLUSIONS

A resistorless beta multiplier current reference design has been proposed in 65 nm CMOS technology which consumes an area of only 0.0031 mm^2. The design uses self-cascode composite MOSFETs in linear region to achieve a low temperature coefficient of 48 ppm/°C. The reference generates an output current of 104.2 nA at supply voltage of 1.33 V with ($3\sigma/\mu$) variation of only 4%. The TC is less than 50 ppm/°C for supply voltage range of 1.285 V to 1.4 V with a line regulation of 1.9 %/V. The circuit has output noise of 12.5 $\mu/\sqrt{Hz}$ at 1 Hz and a PSRR of -63.83 dB at a frequency of 100 Hz. The average power consumption of the circuit is 550 nW. The results illustrate that the proposed design fits the need for modern low power, wireless sensor nodes, energy harvesting, internet of things and biomedical based applications.

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