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Reconfigurable Signal Processing and DSP Hardware Generator for 5G Transmitters

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***Abstract*—To impose the reconfigurability and reusability of digital circuits for millimeterwave transmitter architectures, high-speed digital signal processing architectures are explored. The digital front-end of these next-generation transmitters can be implemented up to the maximum operating frequency to meet the requirements of the 5G NR FR2 frequency bands. This paper presents an efficient implementation of a reconfigurable digital signal processor (DSP) that contains programmable multistage multirate filters, operable up to 4 GHz, and a flexible generator for polar, outphasing, and multilevel outphasing modulation. The system achieves an excellent ACLR of 42 dB and EVM degradation of 1.61% with a 7-bit phase signal at a sampling frequency of 4 GHz for outphasing modulation. Digital synthesis of the circuit in a 22 nm FDSOI process results in a core area of 0.12 mm^2 and an estimated power consumption of 142 mW for a 200 MHz bandwidth 5G NR baseband signal.**

***Index Terms*—Digital signal processing , 5G, System on Chip, Reconfigurable Hardware, Digital Front-end.**

I. Introduction

The next generation of wireless communication systems aims for multi-gigabit/s data rates, ultralow latency, and massive capacity, which is facilitated by a range of low-band, mid-band, and high-band frequency spectrums. To fulfill the requirements of speed and spectrum, programmable digital intensive signal processing units have become standard in hardware technology, as applications in new-age wireless communication systems have outpaced the traditional signal processing capability of analog circuits in terms of increased scalability, reduced cost, and improved performance [1]–[4]. As computational complexity increases with modern communication systems, there is a need to implement a reconfigurable DSP to reduce overhead redesign costs while addressing various processing requirements within the 5G transmitter. Low cost, low power, and the ability to implement a flexible generator targeted toward high-GHz maximum clock frequency for multiple modulation techniques are the requirements to develop a 'one DSP that fits all' over a conventional DSP to support greater functionality on a transmitter chip. Therefore, an algorithmic restructure of traditional DSP-based signal processors is necessary to extend the range and performance of signal processing applications in RF transmitters.

In an operating range of the 5G FR2 frequency band, the need for a reconfigurable signal processing unit with a flexible hardware generator for multi-modulation methods becomes more prominent due to its reusability over multiple transmitter architectures. Thus, an efficient redesign of a configurable DSP unit is needed for multiple modulation techniques while satisfying high-linearity requirements and less error-prone conversions for higher-order signal constellations. This paper presents a reconfigurable signal processing unit with a programmable interpolation chain and a hardware generator for polar, outphasing, and multilevel outphasing transmitter architectures, as seen in Fig. 1. Various programmable options for the DSP in terms of signal upscalability and time multiplexing for multiple modulation techniques were designed in the signal processing architecture to support operation in the 5G NR2 frequency range. However, its functionality has been demonstrated with a 200 MHz. 64 QAM 5G NR baseband signal in the context of outphasing modulation in this work.

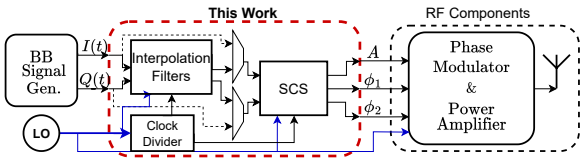

Fig. 1. Configurable DSP between Baseband (BB) Signal Generator and RF Components of a Transmitter.

This paper is organized as follows: Section II presents the signal processing required for upsampling and for polar, outphasing, and multilevel outphasing modulation techniques. The section also describes the architecture used in the configurable DSP unit. Section III describes the hardware implementation of the reconfigurable digital signal processing unit and the flexible hardware generator, also known as the Signal Component Separator (SCS) proposed for the multi-modulation transmitter architecture. This section also highlights the optimization techniques used for area and power efficiency in the DSP unit. Performance metrics in terms of ACLR and EVM, as well as area and power consumption of the DSP processor, are discussed in Section IV. Finally, Section V concludes this paper.

II. Digital Signal Processing for Multi-Modulation Transmitters

In modern transmitters, three types of signal composition are generally applied. Cartesian, Polar and Outphasing.

Cartesian transmitters, which are based on direct modulation of the complex baseband signals, in phase $I(t)$ and quadrature

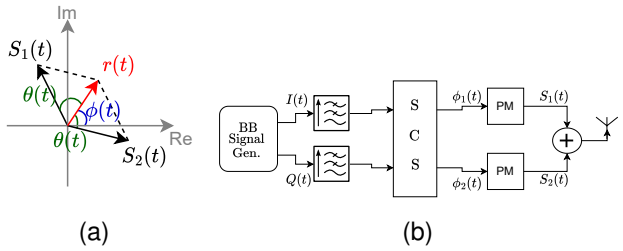

Fig. 2. Outphasing Modulation a) Outphasing vectors in complex plane, b) Generic block diagram of the outphasing transmitter

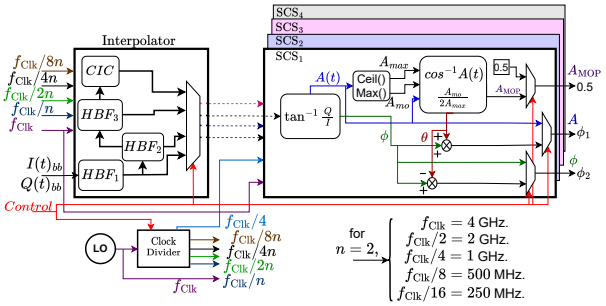

Fig. 3. High Level Functional block diagram of the proposed DSP

signal $Q(t)$, representing the real and imaginary parts of the complex baseband signal.

$$V(t) = I(t) \cdot \cos \omega_c t - Q(t) \cdot \sin \omega_c t, \tag{1}$$

where $V(t)$ is the output signal of the transmitter, ω_c is the angular frequency of the carrier signal.

Cartesian transmitters commonly employ high-resolution D/A conversion for baseband signals, limiting the feasibility of developing a power efficient structure for high-frequency transmitters [5]–[7].

Alternatively in polar transmitters, the complex baseband signal is expressed with amplitude $A(t)$ and phase $\phi(t)$. The relation between the two transmitter architectures are given by

$$A(t) = \sqrt{I(t)^2 + Q(t)^2}, \tag{2}$$

$$\phi(t) = \arctan \frac{Q(t)}{I(t)}. \tag{3}$$

This transmitter architecture is often realized by COordinate Rotation DIgital Computer (CORDIC) algorithm [8], which can be implemented using DSP in the digital domain [9]–[11].

A. Outphasing Modulation

The outphasing modulation technique uses the summation of two complex vectors of constant amplitude with different phase modulation, unlike the traditional Cartesian transmitter, as seen in Fig. 2a. These vectors are represented as [12], [13],

$$S_1(t) = \frac{1}{2} \cos\Big(\omega_c t + \phi(t) + \theta(t)\Big), \tag{4}$$

$$S_2(t) = \frac{1}{2} \cos\Big(\omega_c t + \phi(t) - \theta(t)\Big), \tag{5}$$

$$V(t) = S_1(t) + S_2(t), \tag{6}$$

where $V(t)$ is the modulated RF signal, $S_1(t)$ and $S_2(t)$ are two constant-envelope signals and $\theta(t)$ is outphasing angle defined by the normalized amplitude output $A(t)$ [14],

$$\theta(t) = \arccos A(t). \tag{7}$$

B. Multi-level Outphasing Modulation

To increase power efficiency in the outphasing architecture, which is related to the fundamental limitations of the RF components of a transmitter, multilevel outphasing architecture has been proposed [15]–[17]. Power efficiency is increased by using discrete amplitude levels $A_{MOP}(t)$ and is expressed as

$$V(t) = A_{MOP}(t)(S_1(t) + S_2(t)), \tag{8}$$

where $A_{MOP}(t)$ represents equally spaced discrete amplitude levels [14], and is defined by

$$A_{MOP}(t) = \frac{A_{mo}(t)}{2A_{max}}, \tag{9}$$

$$A_{mo}(t) = \lceil A(t) A_{max} \rceil, \tag{10}$$

where A_{max} is the maximum of discrete amplitude levels.

Fig. 3 shows the two main components of the transmitter DSP: interpolation chain and signal component separator. In this work, we have implemented a programmable interpolator that supports sampling rate conversion ratios up to 128. The input baseband signal is passed through a series of FIR filters to increase the sampling rate before passing through the SCS, given the interpolation factor L. Furthermore, we have implemented a reconfigurable hardware generator for SCS that supports signal component separation for outphasing and polar transmitters. We demonstrate the operation for outphasing transmitters with one amplitude level.

C. Interpolation Filters

In order to perform time-domain interpolation, the input data needs to be up-sampled and then passed to the digital low-pass filters before SCS. Upsampling of a signal by an integer factor of L in the time can be achieved by interpolating $L-1$ samples between successive values of the signal. To eliminate the images of the baseband signal at π/L intervals due to the insertion of $L-1$ zeros at successive samples, a low-pass filter with a frequency response of $H_L(\omega_y)$ is required [18]:

$$H_L(\omega_y) = \begin{cases} C, & 0 \le x \le \pi/L, \\ 0, & \text{otherwise}, \end{cases} \tag{11}$$

where C is scaling factor to normalize the output signal and is equal to L. And $\omega_y = \omega_{bb}/L$ is the interpolated angular frequency and ω_{bb} is the angular frequency of the input baseband signal.

In our implementation of configurable DSP, the sampling rate of the baseband signal $f_{s,bb}$ needs to be interpolated up to 16 times to meet the FR2 frequency range in 5G standards. To

TABLE I
OPERATIONAL FREQUENCY FOR INTERPOLATION FILTERS

Component	Input Frequency	Output Frequency
CIC	$f_{\text{Clk}}/2$	f_{Clk}
HBF_3	$f_{\text{Clk}}/4$	$f_{\text{Clk}}/2$
HBF_2	$f_{\text{Clk}}/8$	$f_{\text{Clk}}/4$
HBF_1	$f_{\text{Clk}}/16 = f_{\text{s,bb}}$	$f_{\text{Clk}}/8$

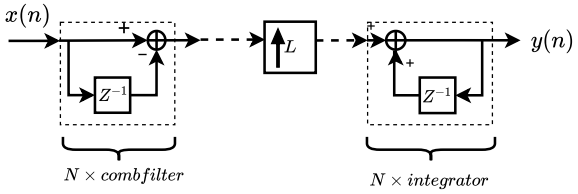

Fig. 4. Cascaded Comb-Integrator filter

achieve the specification, a configurable interpolator chain is used, which consists of three half-band filters (HBF) and one cascaded integrator-comb filter (CIC). In this work, the interpolator is designed to obtain interpolated output at different stages to facilitate different interpolation factors, viz. $2, 4, 8x$, where $x = 1, 2, 3, \ldots, 16$ [19]. A configurable clock divider is also included in the design to provide divided clocks from the $f_{\text{Clk}} = 4$ GHz clock signal. Table I shows the input and output clock frequencies of different stages of the interpolator chain for $n = 2$

1) Half-band FIR Filter: Linear phase half-band FIR filters are used for interpolation applications in multirate filter applications [20]–[22]. In the interpolator chain, to increase the oversampling ratio required by the CIC filter, three half-band filters, each with an interpolation factor of 2 and increasing attenuation stopbands, are cascaded for efficient implementation. In this case, the polyphase implementation of the odd symmetric half-band filter of type II is realized for the area and power efficiency [23].

Fig. 3 shows the functional block diagram of the interpolator, where the output is designed to bypass the different stages of half-band filters, depending on the interpolation factor.

2) Cascaded Comb-integrator (CIC) Filter: Cascaded Comb-integrator filters are computationally efficient linear phase lowpass filters and are often used in interpolation structures [24], [25]. For attenuation of images below 60 dB [26] and a balanced implementation between power consumption, speed, and area, a CIC filter of order $N = 3$ is used in this work.

However, to upsample the input data by an integer factor of L there is a hold unit between the comb filter and the integrator, which holds the value 0 for $L - 1$ samples to increase the sampling rate. As shown in Fig. 4, upsampling is performed after the comb filter to increase power efficiency. The transfer function of the implemented CIC filter is expressed as

$$H(z) = \left[\frac{1 - z^{-L}}{1 - z^{-1}}\right]^3. \tag{12}$$

D. COordinate Rotation DIgital Computer (CORDIC)

CORDIC is a hardware-efficient method that uses iterative rotations to calculate various trigonometric functions with the help of simple operations, that is, add, subtract and shift, while using small LUT [27]. In this work, SCS is used to calculate phase signals from interpolated $I(t)$ and $Q(t)$ signals. Implementing the SCS requires a standard CORDIC module to calculate phase $\phi(t)$, Eq.(3) and amplitude $A(t)$ for polar transmitters, Eq.(2), and a CORDIC-based module to evaluate $\theta(t)$ for outphasing transmitters from Eq.(7). To mitigate the scaling problem of the rotation vector while calculating the inverse cosine, the double iteration algorithm is implemented in this work due to its improved accuracy [28]. The algorithm is given by

$$\begin{pmatrix} x_{n+1} \\ y_{n+1} \end{pmatrix} = \begin{pmatrix} 1 & -d_n 2^{-n} \\ d_n 2^{-n} & 1 \end{pmatrix} \begin{pmatrix} x_n \\ y_n \end{pmatrix} \tag{13}$$

$$\theta_{n+1} = \theta_n + d_n \tanh 2^{-n} \tag{14}$$

$$t_{n+1} = t_n + t_n 2^{-2n} \tag{15}$$

As $n \to 0, 1, 2, 3, \ldots \infty$, then $\theta_n \to \cosh t$, and $\theta_0 = 0, x_0 = 1, y_0 = 0, t_0 = t$ are the initial values for the angle, coordinates of the rotating vector, and input to the inverse cosine function, respectively. The input, $t \epsilon [-1, 1]$ and d_n is defined as

$$d_n = \begin{cases} sign(y_n), & \text{if } x_n \geq t_n. \\ -sign(y_n), & \text{otherwise.} \end{cases} \tag{16}$$

System-level simulations from TheSydekick [29] revealed that an acceptable value of n is 15 for a minimal error rate when calculating the inverse tangent and cosine functions. In the case of outphasing and multi-level outphasing modulation, the output phase signals $\phi_1 = \phi + \theta$ and $\phi_2 = \phi - \theta$, as shown in Eq.(4) needs to rotated from $[-\pi, \pi]$ to $[0, 2\pi]$ to be able to convert it to 7-bit phase signals. This is done by continuously monitoring the sign of the phase signals, and if negative, the resulting phase is summed with 2π as, $\cos(2\pi + \theta) = \cos\theta$. However, Eq.(13) can be simplified to a series of shifts and add operations to reduce the complexity of hardware implementation.

III. DIGITAL SIGNAL PROCESSOR IMPLEMENTATION

This section explores the hardware implementation of signal processing algorithms to extract phase signals from the baseband signals in the case of outphasing/multilevel outphasing modulation. The DSP was implemented and synthesized with a 22 nm FDSOI technology.

The fixed-point implementation of the DSP was designed in CHISEL [30] and simulated with the help of TheSydekick [29] in a Python environment. The master clock frequency of the entire DSP is 4 GHz and is divided internally with the help of a programmable clock divider for multiple clock domains.

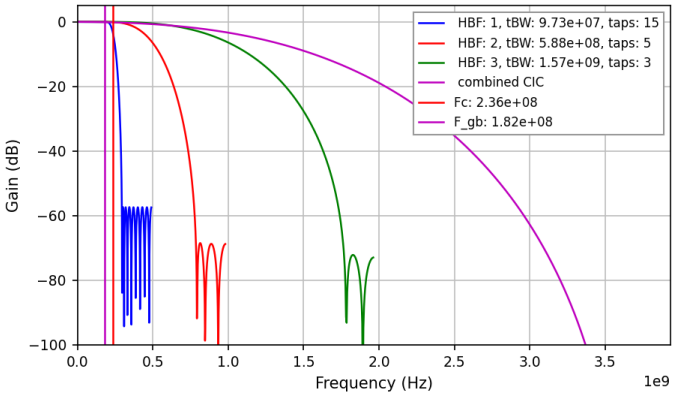

Fig. 5. Frequency Response of Filters

TABLE II
PARAMETERS FOR HALF-BAND INTERPOLATORS

Interpolator	Coeff	Gains	Zeros	Multipliers
1	31	17	14	8
2	15	9	6	4
3	7	5	2	2
Total	53			14

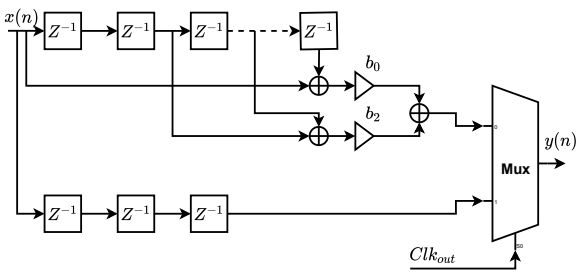

Fig. 6. Hardware Description of HBF

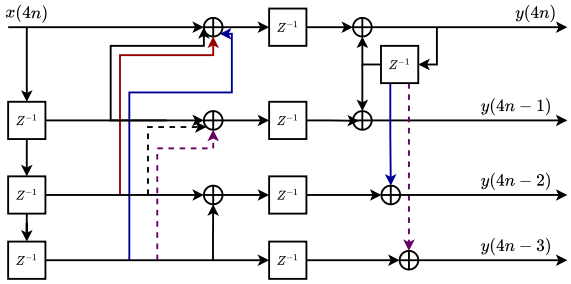

Fig. 7. Unrolling of Integrator by 4

A. Half Band-pass Filters (HBF)

This section describes the design and development of linear phase FIR half-band filters. In our case of designing a sharp cutoff FIR filter with an up-sampling factor of 8, a multi-stage design-based approach has been considered due to its efficiency [21].

Fig. 5 shows the frequency responses of the three cascaded half-band filters and one CIC filter, which have been used in this work. The first half-band filter has a stopband frequency at $\frac{f_s}{8}$, whereas the second and third half-band filters have stopband frequencies at $\frac{f_s}{4}$ and $\frac{f_s}{2}$ respectively. Here f_s is the maximum interpolated sampling frequency of the signal and in this work is at 4 GHz. To increase efficiency in terms of power consumption, a polyphase realization of FIR filters is implemented in the filter architecture, as seen in Fig. 6. This allows us to run the FIR filters at a frequency equal to the input sampling rate. In this work, a suppression of 60 dB for images recurring at $\frac{\pi}{16}$ is achieved. Due to the symmetry of half-band filters around their central coefficient, the number of multipliers can be halved using a direct transpose FIR filter structure. This is expressed as follows:

$$\begin{aligned} H_{hbf3}(z) &= b_0 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + b_4 z^{-4} + b_5 z^{-5} + b_6 z^{-6} \\ &= b_0(1 + z^{-6}) + b_2(z^{-2} + z^{-4}) + z^{-3}, \end{aligned} \tag{17}$$

where $H_{hbf3}(z)$ is the transfer function of the third halfband filter and $b_0, b_1, \ldots, b_6$ are the coefficients of the FIR filter, $b_1 = b_5 = 0$ and $b_0 = b_6$, $b_2 = b_4$, $b_3 = 1$. This odd symmetric nature of halfband FIR filter can reduce the complexity, as shown in Eq.(17) and can be seen in Fig. 6.

Similarly, the other halfband filters ($H_{hbf1}(z)$ and $H_{hbf2}(z)$) were designed using the principle for maximum efficiency of power consumption and area. The total number of required interpolator coefficients and the number of multipliers needed in these half-band filters are listed in Table II.

B. Cascaded Integrator-Comb Filter (CIC)

This section describes the cascaded integrator-comb (CIC) filter used in this work at the last stage of the interpolation chain of the DSP unit.

In this work, we have $N = 3$ stages of cascaded comb filters clocked at $\frac{f_s}{L}$ followed by 3 stages of integrators, running at $f_s = 4$ GHz frequency rate. The transfer function of the 3^{rd} order CIC filter is given by Eq.(12). Since the integrators are running near the operational frequency of digital design, to meet the timing requirements, the integrators have been unrolled by a factor of 4, as seen in Fig. 7. Unrolling is performed as

$$\begin{aligned} y(4n) &= x(4n) + x(4n-1) + x(4n-2) + x(4n-3) \\ &\quad + y(4n-4) \\ y(4n-1) &= x(4n-1) + x(4n-2) + x(4n-3) + y(4n-4) \\ y(4n-2) &= x(4n-2) + x(4n-3) + y(4n-4) \\ y(4n-3) &= x(4n-3) + y(4n-4). \end{aligned} \tag{18}$$

C. Signal Component Separator (SCS)

This section describes the flexible generator for the millimeterwave transmitter, that is SCS. It uses two CORDIC-based algorithms to calculate the amplitude A, A_{MOP} and phase signals ϕ, ϕ_1 and ϕ_2 for multi-modulation technique. In order to increase the performance of SCS, in this work, a pipelined implementation of the 15 stage of the CORDIC algorithm is

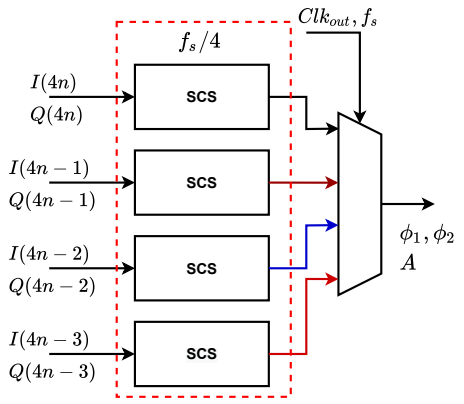

Fig. 8. Time Multiplexing of SCS

implemented rather than feedback structures. The advantage of using a pipelined structure is that it generates output at each clock period at the cost of increased hardware resources. The SCS can be configured for polar, outphasing and multilevel outphasing modulation [15], [31] as seen in Fig. 3.

However, in this work, the functionality of the SCS has been demonstrated only in the context of outphasing modulation. The output phase signals ϕ_1 and ϕ_2 in this work are converted to 7-bit phase signals by multiplying ϕ_1 and ϕ_2 with a constant factor of 201.06 ($128/2\pi$), to facilitate the RF components in a transmitter. In this work, the SCS is required to perform complex mathematical operations to calculate the phase and amplitude signals for multiple modulation techniques, at high speed (4 GHz). To meet the timing requirements of the said design, the SCS needs to be time-multiplexed to execute at high speed. Fig. 8 shows the architecture of the time-multiplexed SCS, where the SCS is running at $\frac{f_s}{4}$ = 1 GHz. The output data is provided by a multiplexer running at 4 GHz at the output of the module.

IV. Simulation Results

This section discusses the performance of the implemented hardware of the proposed design in the 22 nm FDSOI technology. The system is fed with a 16-bit, 200MHz bandwidth 5G NR FR2 baseband signal to leave sufficient space for non-idealities of the RF front-end [20]. The performance of the system is evaluated on the error vector magnitude (EVM) and adjacent channel leakage ratio (ACLR) of the transmitted signal. Fig. 9 shows the ACLR and EVM performance of the DSP, operating at an output frequency of 4 GHz. The hardware resource utilization and power consumption of the proposed design will also be discussed later in this section.

A. Baseband Signal Input

Baseband (BB) signal in compliance with 5G communication standards was generated using a BB signal generator. To feed these normalized in-phase and quadrature signals (I and Q) as a 16-bit input to the hardware, it needs to be scaled to fit the 16-bit value, including the sign (±) bit.

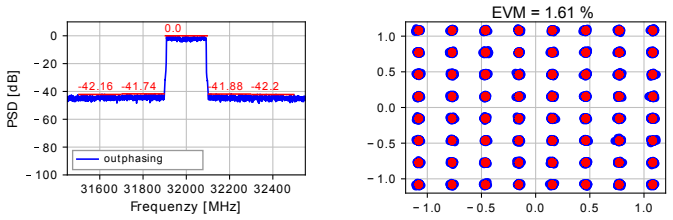

Fig. 9. a) ACLR & b) EVM performance of hardware DSP for an interpolation factor of 16

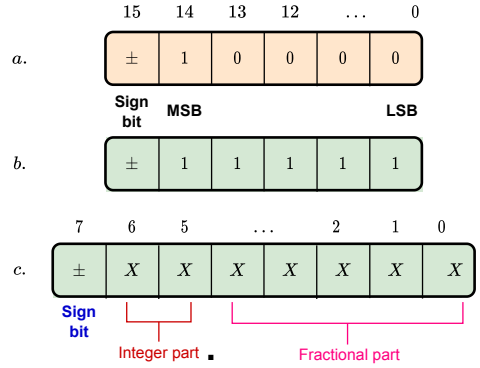

Fig. 10. Input data scaling a) Scaling used in this work, b) Full bit scaling, and c) Representation of fixed-point scaling with separate integer and fractional part of a given number.

Fig. 10 shows the scaling of the input data used in this work. To represent the fractional number 0.99 in the binary notation of 15-bit, full-bit scaling (Eq.(19)) requires more bits to charge from 0 → 1 than our integer scaling method (Eq.(20)). This method results in 10% less switching of load capacitors for our input baseband signal, which facilitates low-power design.

$$0.99 \rightarrow \times(2^{15}-1) = (32439.3)_{10} = (111111010110111)_2 \quad (19)$$

$$0.99 \rightarrow \times(2^{14}) = (16220.1)_{10} = (011111101011100)_2 \quad (20)$$

B. Error Vector Magnitude (EVM)

The EVM evaluation for the outphasing modulation of the DSP model uses a 200 MHz 64QAM 5G NR signal as input signal. In this case, the DSP is also evaluated for different interpolation factors, that is, 16, 8, 4. Finally, in Table III, we compare the DSP for both the ideal Python-based software model (S/W, Sydekick [29]) and the hardware model (H/W) for different interpolation factors.

C. Adjacent-Channel Leakage Ratio (ACLR)

Table IV shows the lower adjacent channel leakage ratio ($ACLR_1$) and higher adjacent channel leakage ratio ($ACLR_2$) to the center frequency for both the software and hardware model of the proposed DSP. Similar to the EVM measurement, we also compare the DSP for both the ideal Python-based software (S/W) and the hardware (H/W) model for different interpolation factors.

TABLE III
EVM CALCULATION OF SOFTWARE(S/W) AND HARDWARE(H/W) MODEL OF THE DSP

Modulation Type	**Interpolation factor**	**EVM** (S/W)	**EVM** (H/W)
Outphasing	16	1.55%	1.61%
Outphasing	8	3.12%	2.58%
Outphasing	4	5.58 %	5.04%

TABLE IV
ACLR PERFORMANCE OF SOFTWARE(S/W) AND HARDWARE(H/W) MODEL OF THE DSP

Interpolation factor	$ACLR_1$ (dB)		$ACLR_2$ (dB)	
	(S/W)	(H/W)	(S/W)	(H/W)
16	41.6, 41.7	41.7, 41.9	41.9, 42	42.2, 42.2
8	41.6, 41.7	41.8, 41.8	42, 42	42.1, 42.1
4	41.4, 41.5	41.7, 41.8	41.2, 41.1	41.4, 41.5

D. Hardware Utilization

The utilization of hardware resources in digital design is one of the important design parameters, as most of the time the synthesis and place and route of an algorithm implemented are handled by an automated tool.

The implementation of this proposed DSP processor was synthesized in a 22 nm FDSOI technology node. The results are summarized in Table V. Although, as can be seen in Table V, the area consumption has increased with SCS since it contains 4 times the number of hardware resources than a single SCS instance. This is due to the proportionally lower sampling frequency used in the individual SCS component, as mentioned in Section III-C.

E. Power Consumption

In DSP applications, most of the power is lost in the multipliers and sequential elements in a high-speed design. To reduce power consumption at high operating frequency, we optimize interpolation filters and SCS to accommodate fewer multipliers and sequential units. However, to meet the timing constraints in high-frequency operation, some part of the DSP, that is, the SCS had to be replicated four times to use the benefit of multiplexing in the time domain at the cost of increased hardware resources, as seen in Table V.

To the author's knowledge, there is very little information about the power-to-performance parameters of the digital front end of an outphasing transmitter. Table VI shows the performance metrics of the DSP (baseband only) in this work, compared to the prior art of the related transmitter architecture.

TABLE V
HW UTILIZATION OF SYNTHESIZED CIRCUIT

Post-synthesis utilization estimates (summary)		
Instamce Name	Instance Count	Total Area (μm^2)
Interpolator	1	28595.97
SCS	4	95296.68
Total	-	123552.1

TABLE VI
DSP PERFORMANCE COMPARISON WITH PRIOR ARTS

Prior Arts	**CMOS Process**	**Architecture**	**Frequency** (GHz)	**Power** (mW)
Y. Liu et al. [32]	55nm	Digital polar	0.19	12
G. S. Franco et al. [33]	28nm	Outphasing	1.96	57.2* *SCS only
J. Lemberg et al. [34]	28nm	Triphasing	1.9	189
This Work	22nm FDSOI	Multi-modulation	4	142

V. CONCLUSION

This paper proposes a low-power, high-speed design of a programmable digital signal processor with a flexible generator for multi-modulation transmitters. The proposed DSP provides filtering to the sampling images due to upsampling of the baseband signal and converts them to amplitude and phase signals for polar, outphasing, and multilevel outphasing modulation. The DSP is synthesized in a 22 nm FDSOI technology node, and achieves an EVM of 1.61% and an ACLR of −42 dB for outphasing modulation with a 200 MHz 5G NR baseband signal, with an output sampling rate of 4 GHz. The proposed hardware consumes about 33% less power than the known prior art, which contains a configurable DSP, clock divider, and SPI engine to feed data. In addition to being configurable for multiple signal modulations, it can also be configured to have an output sampling rate up until 128 compared to the baseband frequency. Therefore, the DSP in this work is an enabler of next-generation millimeterwave transmitters for 5G communication systems.

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