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Provision of Synthetic Inertia Support for Converter-Dominated Weak Grids

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Abstract—Insufficient inertia is the paramount challenge in power system transition toward 100% converter-based generation. A promising solution to this issue is utilizing distributed virtual inertia (DVI) concept, i.e., releasing energy stored in the dc-link capacitors of power converters employed in the grid following a frequency disturbance. Nevertheless, this method has two drawbacks: 1) the dc-link voltage is not reverted to its reference value after the power mismatch between generation and demand, and 2) it yields instability of a local mode associated with the control system when the converter operates in weak grids. To overcome the aforesaid problems, the conventional DVI loop is modified so as not to affect the outer loop voltage regulator after transient. Moreover, an efficient compensator is presented in this article which eliminates the adverse impact of DVI technique on the converter stability in weak grid connections. The efficacy of proposed control scheme is depicted by simulations in MATLAB. The results illustrate that an improvement of 23% is evident in the grid frequency rate of change following a frequency contingency collated with the case in which the DVI loop staying nullified.

Index Terms—Distributed virtual inertia, phase-locked loop (PLL) dynamics, power converter, primary frequency regulation, weak grid.

NOMENCLATURE

Abbreviations

DVI	Distributed virtual inertia.
PoI	Point of interconnection.
RESs	Renewable energy sources.
RoCoF	Rate of change of frequency.
SG	Synchronous generator.
SRF	Synchronous reference frame.
SCR	Short-circuit ratio.

Variables

i	Grid current space vector.
i_w	Converter current space vector.
p_{out}, q_{out}	Converter output power.
u_g	Grid voltage space vector.
u_p	PoI voltage space vector.

u_t	Converter voltage space vector.
u_{dc}	DC-link capacitor voltage.
ω	Grid angular frequency.
δ	Synchronization angle.
<i>Parameters</i>	
C_{dc}, C_f	DC-link capacitor, filter capacitor.
k, k_d	DVI gain, compensator gain.
k_{pll}, k_{ipll}	PLL controller gains.
k_{pi}, k_{ii}	Current controller gains.
k_{pu}, k_{iu}	Voltage controller gains.
k_{pf}	Voltage recovery gain.
i_w^*	Converter current reference space vector.
R_f, R_g	Filter resistance, grid resistance.
L_f, L_g	Filter inductance, grid inductance.
u_{dc}^*	DC-link voltage reference.
ω_0	Grid nominal angular frequency.
ω_d	Compensator cut-off frequency.
ζ_d	Compensator damping ratio.
<i>Indices</i>	
$dq-$	Grid synchronous reference frame.
dq^c-	Control synchronous reference frame.

I. INTRODUCTION

THE current energy arena is changing, from fossil fuel-based generation to power electronic converter interfaced renewable generation. Hence, the power system inertia and short-circuit current gradually reduce [1]. The inherent inertia of synchronous machine acts as the first response to frequency events (e.g., any mismatch in the supply–demand balance) by providing or absorbing kinetic energy to or from the grid. This characteristic slows down grid frequency dynamics [2], [3]. In contrast, converter-based generators fundamentally have no rotational inertia of synchronous generator (SGs), thus, making power grid more sensitive to frequency perturbation and jeopardizes system stability [4], [5].

The main performance indices: 1) the maximum rate of change of frequency; and 2) frequency nadir—the minimum frequency reached following a disturbance assess grid frequency stability. The overall system inertia is the major factor affecting the aforesaid indices during a transient; i.e., the more inertia, the better primary frequency regulation [6], [7]. On the other hand, diminution of system inertia limits further increases in renewable energy sources (RESs) penetration [8]. This is because RESs integrating into the network through power converters

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do not inherently contribute to the system inertia. To address this issue, synthetic inertia concept (defined as the contribution of a converter-based generator to emulate the inertial response of real SGs [9], [10]) has been proposed through a plethora of mechanisms; i.e., readjusting converter power reference in response to disturbances, which is analogous to the kinetic energy released or absorbed by the SGs.

A. Review of Relevant Works

The mainstream synthetic inertia techniques with/without energy storage are categorized as follows: 1) synchronous condensers (SCs); 2) virtual synchronous machines (VSMs); 3) wind turbines; 4) ultracapacitors (UCs); 5) batteries; and 6) dc-link capacitors [11]. A simple solution for power system inertia enhancement is employing backup SGs with partial loading,—i.e., spinning reserve—or SCs to provide more rotating masses. Nonetheless, these approaches yield high capital and operating cost [11]. Motivated by SG dynamics, Beck and Hesse [12] introduce VSM that contributes to stabilization of the grid frequency. Renewable generators augmented with this device can operate as electromechanical SGs regarding reaction to transients. The analogous approach, so-called synchronverter, is developed in [13] as well. The dynamic equations governing a synchronverter are the same as real SGs; only the mechanical power exchanged with the prime mover is replaced with the power exchanged with the inverter dc bus. Hence, a synchronverter has all the merits and demerits of an SG. For example, loss of stability due to underexcitation and oscillations around the synchronous frequency could occur in a synchronverter. An advantage of VSM and synchronverter compared to SG is that we can change the virtual inertia value. Akin to conventional generators, wind turbines enjoy a considerable amount of kinetic energy preserved in their blades. In conventional variable-speed wind turbines (viz doubly fed induction generators or permanent magnet SGs), however, this energy does not contribute to grid inertia due to the converter interface [14]. Multiple control mechanisms have been proposed to enable aforesaid generators providing inertial response. A modified controller is presented in [15] that adapts the turbine torque set point as a function of the time derivative of frequency (df/dt) and frequency deviation (Δf), enabling wind turbine to emulate inertia. However, df/dt loop can induce instability to the converter controller as depicted in [16]. Notably, the synthetic inertia of wind turbines is limited by converter power rating, speed, recovery period, etc. [17]. Over recent years, grid-scale energy storage systems (ESSs) gained popularity in power system for dynamic frequency regulation and ramp-rate mitigation of renewable generators. Sockeel *et al.* [18] apply virtual inertia emulator-based model predictive control for an ESS-fed inverter in a power system dominated by RESs aimed at grid frequency regulation. This article uses small prediction horizon of 1, which does not guarantee optimal control operation [19]. Kakimoto *et al.* [20] employ an UC to absorb rapid fluctuations of a photovoltaic generator, leading to change its output at a limited ramp rate. One disadvantage of this method is that it requires measuring of the generator output power, which restricts the location of the UC or establishes the

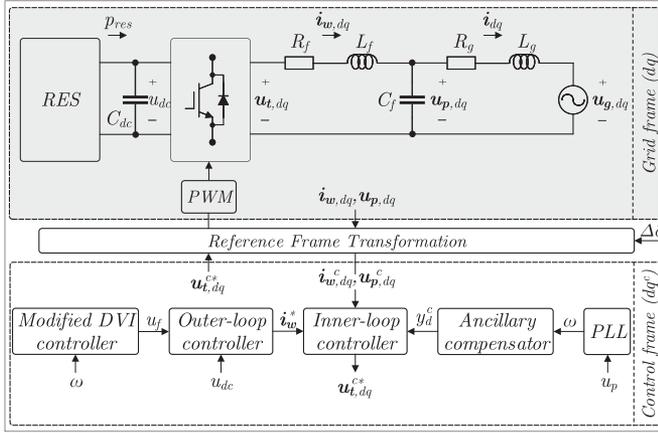
need for a communication link to transmit the measurements [21]. Tan *et al.* [22], suggest integrating a multilevel storage system, composed of UCs and lead-acid batteries (LABs), into dc-side of permanent magnet SG wind farms. The UC deals with fast-changing frequency by providing synthetic inertia through df/dt -based approach (which it is prone to instability [16]), while the LAB mimics automatic governor response. Datta *et al.* in [23], introduced a droop-type, lead-lag controlled battery EES with a new adaptive state-of-charge recovery. This method enhances inertial and damping ability of the host power system. An emerging technique named distributed virtual inertia (DVI) for inertia emulation via power converters is proposed in [11], [24], and [25]. This method applies dc capacitance adhered to the dc-link of grid-tied power converters (e.g., employed in renewable generators, variable-speed drives, active power filters, switched-mode power supplies, etc.) as the energy buffer for frequency stability enhancement. In other terms, the emulated inertia through the DVI technique is generated with a large number of capacitors utilized in many power converters distributed in future power grids. The DVI concept can be easily implemented without increasing system cost and complexity.

B. Motivations and Contributions

In conventional DVI-based grid-interactive converter, the dc-link voltage is not restored to its nominal value after providing synthetic inertia unless the grid supply—demand balance holds true [24]. Also, the small-signal stability analysis discloses that the gain of DVI function induces instability to the converter controller under weak grid connections. The higher DVI gain, the better transient grid frequency response after frequency perturbation; however, it deteriorates the converter stability. Hence, to address the aforesaid issues, the contributions of this article to the research field are summarized as follows.

- 1) The DVI loop is modified to a frequency-dependent function so as its output starts converging to zero when the grid frequency reaches recovery and quasi-steady sections (i.e., from the frequency nadir onwards). Thus, the dc-bus voltage is recovered to its reference after the frequency disturbance.
- 2) A second-order compensation technique is proposed and designed. The compensator output introduces one-degree-of-freedom to the direct axis current controller, by which the adverse impact of the DVI gain on the converter stability is eliminated.

The remainder of the article is organized as follows. Section II presents the grid-interfaced converter control scheme augmented with the modified DVI function. The state-space model of the system is derived in Section III. Then, the eigenvalue analyses aimed at evaluating the sensitivity of the control parameters and DVI gain on system stability are provided in Section IV. The ancillary compensator and its design process are discussed in Section V. The efficacy of the proposed control framework is demonstrated in Section VI by simulations. Finally, the article ends with conclusion in Section VII.

Fig. 1. Grid-connected converter model in dq -coordinates.

II. CONTROL CONFIGURATION

Throughout this article, the entire modeling, analysis, and control of the voltage-sourced converter is implemented in the synchronous reference frame (SRF), in which quantities are written in complex space vectors—denoted with boldface letters, – e.g., $\mathbf{u}_g = u_{gd} + j u_{gq}$ for the grid voltage. Moreover, the control commands and set points are marked with “*” in superscripts. Consider Fig. 1. The quantities in the three-phase side are expressed in the grid dq -coordinate. An LC converter output filter is assumed to mitigate high-order harmonics introduced by the switching process. The voltage source u_g in series with the line impedance Z_g serves as the grid model with the stiffness defined by short-circuit ratio as

$$SCR = \frac{u_{p,rated}^2 / Z_g}{p_{out,rated}}. \quad (1)$$

The network with $SCR \geq 3$ defines a strong grid, whereas $SCR < 3$ represents a weak grid condition [26]. Herein, we consider $SCR = 2$. On the dc side, C_{dc} is the dc capacitance acting as the energy buffer in the DVI technique for transient frequency stability enhancement. The mechanism of providing synthetic inertia through this approach is as follows: any frequency oscillation ($\Delta\omega = \omega_0 - \omega$) raised by the power imbalance between generation and demand is proportionally connected to the outer loop voltage control, i.e., $u_f = k\Delta\omega$. The relevant control architecture is later detailed in Fig. 4. Hence, the ancillary signal u_f yields discharging (charging) C_{dc} , which is analogous to the released (absorbed) kinetic energy by SGs during frequency disturbance. The synthetic inertia coefficient provided by the dc-link capacitor under a certain converter power rating $V A_{rated}$ is expressed as [11], [24]

$$H_{cap} = k \frac{C_{dc} u_{dc}^{*2}}{2V A_{rated}}. \quad (2)$$

Notably, H_{cap} is limited by the dc capacitance and the maximum acceptable dc-side voltage change. The later one can be improved via injecting third-harmonic term into modulating reference [27]. The candidate applications of grid-tied power converters augmented with the DVI function are solar and wind

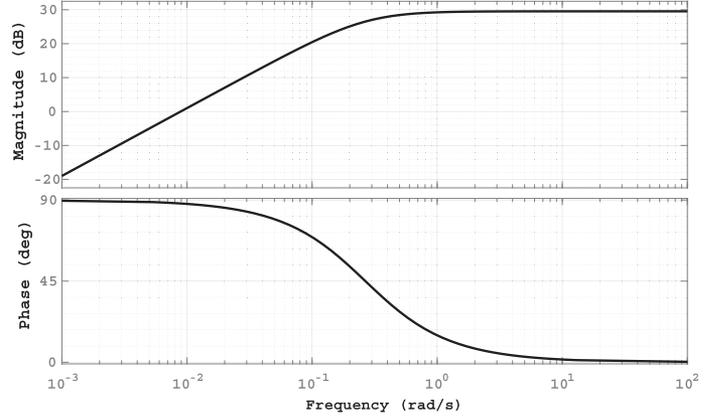
Fig. 2. Frequency response of $G_f(s)$.

TABLE I
CONVERTER AND GRID PARAMETERS

Parameter	Value	Parameter	Value
R_f, R_g	0.1 Ω , 2.5 Ω	k_{ppll}, k_{ipll}	15, 300
L_f, L_g	2.94 mH, 10 mH	k_{pi}, k_{ii}	1.176, 470.4
C_f, C_{dc}	50 μ F, 5 mF	k_{pu}, k_{iu}	0.1, 5
k, k_d	30 Vs, 3.2 Vs	u_{dc}^*	750 V
k_{pf}	1 FV/s	ω_0	$2\pi \times 50$ rad/s
ζ_d	0.8	$V A_{rated}$	20 kVA
ω_d	800 rad/s	$u_{p,rated}$	400 V

generators, energy storage systems, active power filters, variable speed drives, static volt-ampere reactive (VAR) compensators, and modular multilevel converters (MMCs) employed in high-voltage direct current systems [11].

Nonetheless, the aforesaid correlation does not restore the dc-link voltage to its nominal value until the supply–demand balance holds true. Furthermore, the converter cannot provide multiple inertia support in case of cascading frequency events. This is because the dc voltage drifts into lower value in each operation, which undesirable over modulation may arise. To address this issue, u_f should start converging to zero as the grid frequency reaches recovery and quasi-steady sections (i.e., from the frequency nadir onwards). To this end, the ancillary signal u_f is modified as

$$u_f = k\Delta\omega - \underbrace{k_{pf} \int \frac{u_f}{C_{dc} u_{dc}^*} d\tau}_{\varphi_f}. \quad (3)$$

resulting in the transfer function of

$$G_f(s) = \frac{u_f}{\Delta\omega} = k \frac{s C_{dc} u_{dc}^*}{s C_{dc} u_{dc}^* + k_{pf}}. \quad (4)$$

Fig. 2 depicts the frequency response of $G_f(s)$, in which the parameters are set according to Table I. Assume a grid frequency disturbance occurs. The grid frequency—including high-frequency (HF) components—then falls (or rises), which is passed through $G_f(s)$; i.e., $\Delta\omega$ is multiplied by 29.55 dB, just equal to $k = 30$ Vs. As the grid frequency reaches recovery and quasi-steady sections (moving towards low- and zero-frequency

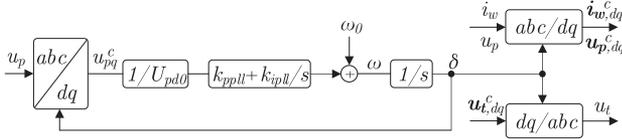


Fig. 3. SRF-PLL structure.

components, respectively), $G_f(s)$ starts decreasing to zero (cf. Fig. 2). Thus, the dc-link voltage regains its nominal as u_f becomes zero.

III. SYSTEM MODELING

This section includes the nonlinear mathematical model for each control block and system element shown in Fig. 1. Subsequently, the equations are linearized around equilibrium points, denoted by “0” in subscripts, to establish a small-signal state-space model [28].

A. Phase-Locked Loop

The synchronization of converter with the network is procured by a phase-locked loop (PLL). Due to the PLL dynamics, the system depicted in Fig. 1 embodies two SRFs [29], [30]: one is grid frame (dq) and the other is control frame (dq^c). The former one is defined by the point of interconnection (PoI) voltage whilst the synchronization angle δ from the PLL introduces the latter one. The dq^c frame coincides with the grid dq coordinate in the steady state. However, when a grid frequency disturbance occurs, the angle δ oscillates to resynchronize the converter with the grid. Hence, the frames are no longer aligned and dq^c lags the grid frame by $\Delta\delta$. The relation between two frames, e.g., for the PoI voltage, is established as

$$\mathbf{u}_p^c = e^{-j\Delta\delta} \mathbf{u}_p. \quad (5)$$

Assume a second-order PLL [31] is employed to drive the q -part of the PoI voltage in the control dq frame to zero (cf. Fig. 3). The state-space representation of the PLL is obtained as

$$\dot{\delta} = \omega = \omega_0 + \frac{k_{ppll}}{U_{pd0}} u_{pq}^c + \underbrace{\frac{k_{ipll}}{U_{pd0}} \int u_{pq}^c dt}_{\varphi_\delta}. \quad (6)$$

It is noteworthy that vectors in the control coordinate are marked with “ c ” in superscripts. Thus, the following process is implemented in the control system to accurately model the PLL dynamics: the measured quantities \mathbf{i}_w and \mathbf{u}_p in the grid SRF are rotated to the converter SRF for feedback control. Then, the voltage command \mathbf{u}_t^{c*} generated by the control loops is retransformed to the grid coordinate (i.e., $\mathbf{u}_t^{c*} \rightarrow \mathbf{u}_t^*$). Assuming $\Delta\delta$ is small enough, the aforesaid procedure can be mathematically expressed as

$$\begin{aligned} \mathbf{i}_w^c &= (1 - j\Delta\delta) \mathbf{i}_w, \quad \mathbf{u}_p^c \\ &= (1 - j\Delta\delta) \mathbf{u}_p, \quad \mathbf{u}_t^* = (1 + j\Delta\delta) \mathbf{u}_t^{c*}. \end{aligned} \quad (7)$$

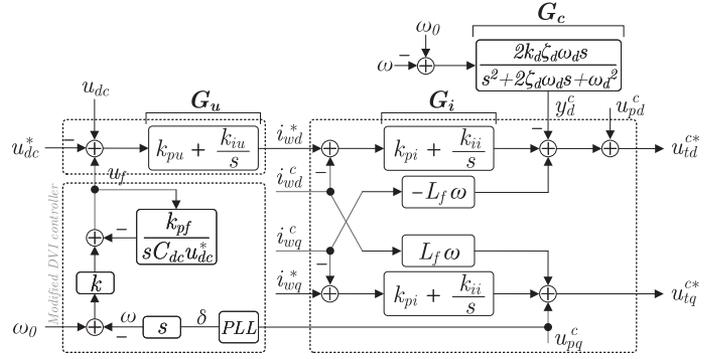


Fig. 4. Grid-following control architecture with modified DVI technique.

B. DC-Side Dynamics

We neglect the energy loss in the converter and interfaced filter. Thus, the state-space realization of the dc-link dynamics based on the power balance between two sides of the converter is attained as

$$\dot{u}_{dc} = \frac{p_{in} - \frac{3}{2}(u_{pd}i_{wd} + u_{pq}i_{wq})}{C_{dc}u_{dc}}. \quad (8)$$

C. AC-Side Dynamics

The converter ac-side includes an LC filter and electric system. The grid is modeled as Thevenin equivalent. This simple structure is applied to obtain a basic model focusing on the dynamics of the converter rather than ac network topology. Without major inaccuracy, it is assumed that the voltage command \mathbf{u}_t^* generated by the feedback loops appears at the input side of the filter (i.e., $\mathbf{u}_t^* = \mathbf{u}_t$). This approach only ignores the power loss across converter switches [32]. The state-space equations governing the ac-side dynamics are expressed in the grid SRF as

$$\dot{\mathbf{i}}_w = \frac{1}{L_f} \mathbf{u}_t - \frac{1}{L_f} \mathbf{u}_p - \left(\frac{R_f}{L_f} + j\omega \right) \mathbf{i}_w \quad (9)$$

$$\dot{\mathbf{u}}_p = \frac{1}{C_f} \mathbf{i}_w - \frac{1}{C_f} \mathbf{i} - j\omega \mathbf{u}_p \quad (10)$$

$$\dot{\mathbf{i}} = \frac{1}{L_g} \mathbf{u}_p - \frac{1}{L_g} \mathbf{u}_g - \left(\frac{R_g}{L_g} + j\omega \right) \mathbf{i}. \quad (11)$$

D. AC Current Control

A set of proportional–integral (PI)-controllers are employed for the inner loop current control, as illustrated in Fig. 4. It regulates the converter current \mathbf{i}_w to its reference value $\mathbf{i}_w^* = i_{wd}^* + j i_{wq}^*$. The PoI voltage feedforward and cancelation of the dq -cross-coupling is also considered [29]. Using complex-valued space vector presentation, the voltage command \mathbf{u}_t^{c*} in the control SRF is expressed as

$$\mathbf{u}_t^{c*} = \mathbf{u}_p^c + j\omega L_f \mathbf{i}_w^c$$

$$+ k_{pi}(\dot{\mathbf{i}}_{\mathbf{w}}^* - \dot{\mathbf{i}}_{\mathbf{w}}^c) + \underbrace{k_{ii} \int (\dot{\mathbf{i}}_{\mathbf{w}}^* - \dot{\mathbf{i}}_{\mathbf{w}}^c) dt}_{\varphi_{i_{\mathbf{w}},dq}}. \quad (12)$$

The signal \mathbf{u}_t^{c*} is first transformed to the grid coordinate (i.e., $\mathbf{u}_t^{c*} \rightarrow \mathbf{u}_t^*$) and then applied to pulsewidth modulation (PWM) block. The converter reference current $\dot{\mathbf{i}}_{\mathbf{w}}^*$ is always expressed in the control coordinate. Hence, it is not remarked with “c” in superscript. Notably, the d -axis current reference is obtained from the dc voltage regulator described in following subsection, whilst reactive power requirement determines the q -axis current reference [33].

E. DC Voltage Control

The dc-link voltage is set to its nominal value by a PI-controller. Moreover, the ancillary signal u_f generated by the modified DVI technique is added to the dc voltage control. This signal aims at enhancing grid frequency stability indices (i.e., RoCoF and frequency nadir). Hence, the state equation describing the voltage controller is

$$\dot{i}_{wd}^* = k_{pu}[u_{dc} - u_{dc}^* - u_f] + \underbrace{k_{iu} \int [u_{dc} - u_{dc}^* - u_f] dt}_{\varphi_u} \quad (13)$$

in which u_f is expressed as (3). Remarkably, the dc-side voltage must be limited within $u_{dc}^{\min} \leq u_{dc} \leq u_{dc}^{\max}$. The lower bound is to ensure the linear modulation of the converter. In contrast, the voltage rating of active and passive elements determines the upper bound u_{dc}^{\max} . Thus, the signal u_f must be restricted so that the dc-link voltage holds the aforesaid range.

IV. STABILITY ASSESSMENT

This section provides stability analyses of the grid-tied converter illustrated in Fig. 1. The study is based on eigenvalues from the small-signal model of the system. Therefore, the state equations (3)–(13) are linearized around an operating point to obtain standard small-signal state-space form

$$[\Delta \dot{x}_{\text{uncomp}}] = [A_{\text{uncomp}}][\Delta x_{\text{uncomp}}] + [B_{\text{uncomp}}][\Delta u] \quad (14)$$

where the subscript “uncomp” stands for uncompensated system. The state vector Δx_{uncomp} and the input vector Δu are defined, respectively, as

$$\Delta x_{\text{uncomp}} = [\Delta \delta \ \Delta \varphi_\delta \ \Delta i_{wd} \ \Delta i_{wq} \ \Delta u_{pd} \ \Delta u_{pq} \ \Delta u_{dc} \ \Delta \varphi_u \ \Delta \varphi_{i_{wd}} \ \Delta \varphi_{i_{wq}} \ \Delta i_d \ \Delta i_q \ \Delta \varphi_f]_{1 \times 13}^T \quad (15)$$

$$\Delta u = [\Delta p_{\text{res}} \ \Delta i_{wq}^*]_{1 \times 2}^T. \quad (16)$$

The corresponding state and input matrices are provided in Appendix A. Moreover, the specifications of system under study are tabulated in Table I. Hereafter, we study the sensitivity of stability in terms of main control parameters. Fig. 5(a) depicts the eigenvalue locus of the uncompensated system with SCR = 2 when the DVI gain k is set to zero (i.e., the DVI loop

is nullified). The eigenvalues define seven distinct modes. As per the Lyapunov stability theory and Fig. 5(a), the system is asymptotically stable in the small-signal sense. Fig. 5(b)–(e) shows four case studies, modifying the parameters of 1) inner current control, 2) outer voltage control, 3) PLL unit, and 4) DVI control, respectively.

In case 1, the PI control parameters are scaled using the variable α_i , which is increased from 0.1 to 2 with variations of 0.1. The modification of current control parameters affects modes 6 and 7. The remaining poles are scarcely sensitive to the current control variation. As observed from Fig. 5(b), increasing α_i yields movement of modes 6 and 7 toward the left-hand side of s -plane. In case 2, the voltage control parameters are scaled by α_u , which varies between $0.1 \leq \alpha_u \leq 2$ [cf. Fig. 5(c)]. Manifestly, only modes 1, 2, and 5 are not sensitive to voltage control variation. Nonetheless, the system is stable as all the poles remain in the left-half plane. The modification of PLL parameters with multiplying the variable $0.1 \leq \alpha_{pll} \leq 2$ is illustrated in Fig. 5(d). It is observed that the control system without DVI loop is robust against changes in the PLL gains if α_{pll} holds the aforesaid range.

When the DVI function is activated in case 4 with increasing the gain k , the local mode 4 is prone to become unstable. The higher DVI gain, the better short-term frequency regulation; nonetheless, it deteriorates the system stability as illustrated in Fig. 5(e). It is worth pointing out that the converter remains stable even with high DVI gain when the grid is strong enough. Fig. 5(f) demonstrates the eigenvalue loci of the converter operating in two different SCR conditions. It is clear that the system is stable with $k = 26$ when SCR = 5, whilst it subjects to instability in weaker grid with the same k .

V. ANCILLARY COMPENSATION TECHNIQUE

A. Model Description

The preceding small-signal analyses affirmed that the DVI loop (aimed at synthetic inertia provision) induces instability to the converter operating in weak grids. To overcome this problem, an auxiliary compensator is hence presented in this section. The compensator output $y_d^c(s)$ is added to the d -axis inner current control, as depicted in Fig. 4, and it is modeled in Laplace domain as

$$y_d^c(s) = \underbrace{\left(\frac{2k_d \zeta_d \omega_d s}{s^2 + 2\zeta_d \omega_d s + \omega_d^2} \right)}_{G_c(s)} \Delta \omega. \quad (17)$$

The following process is performed to obtain $y_d^c(s)$: the time-derivative of synchronization angle (i.e., $\dot{\delta}$ or ω) is first measured. This is because the signal ω entered to the d -channel via the DVI loop is the detrimental factor to the converter stability and must be utilized to mitigate the adverse impact of the DVI gain. Remarkably, the compensator must not affect the tracking of controlled variables in steady state (i.e., when $\omega = \omega_0$). This aim is achieved by applying the term $\omega_0 - \omega$ as

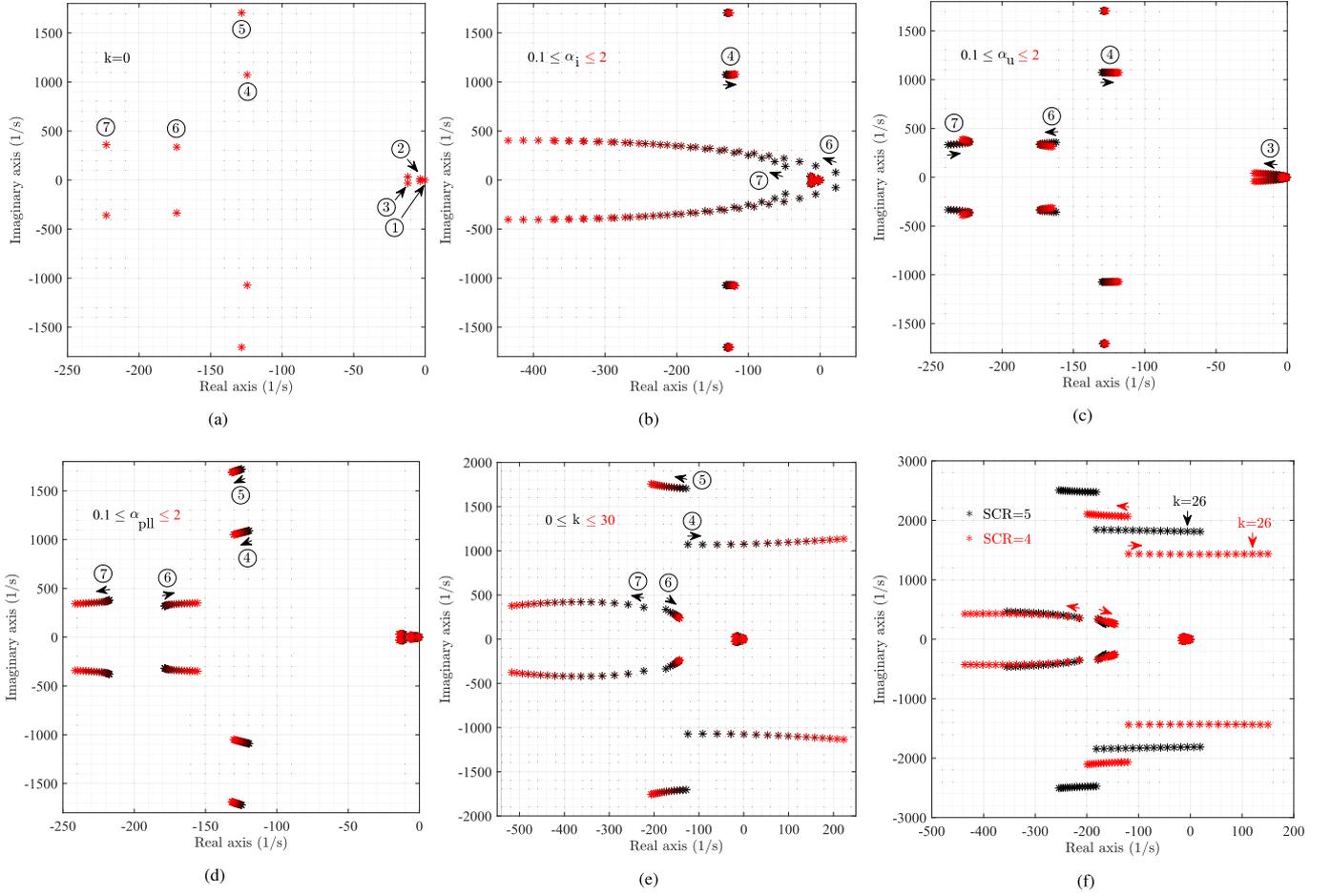


Fig. 5. Pole diagram of the uncompensated converter (a) $k = 0$, (b) $0.1 \leq \alpha_i \leq 2$, (c) $0.1 \leq \alpha_u \leq 2$, (d) $0.1 \leq \alpha_{pll} \leq 2$, (e) $0 \leq k \leq 30$, and (f) different SCRs.

the input signal to (17), which is then passed through a bandpass filter to attain $y_d^c(s)$. The parameters k_d , ζ_d , and ω_d associated with the employed filter are the gain, damping ratio, and cut-off frequency, respectively.

The applied compensator introduces two state variables, γ_1 and γ_2 , with the small-signal state-space representation as

$$\begin{aligned} \begin{bmatrix} \Delta \dot{\gamma}_1 \\ \Delta \dot{\gamma}_2 \end{bmatrix} &= \begin{bmatrix} -2\zeta_d\omega_d & 1 \\ -\omega_d^2 & 0 \end{bmatrix} \begin{bmatrix} \Delta \gamma_1 \\ \Delta \gamma_2 \end{bmatrix} + \begin{bmatrix} -2\zeta_d\omega_d k_d k_{ppll} \\ 0 \end{bmatrix} \Delta \delta \\ &+ \begin{bmatrix} 2\zeta_d\omega_d k_d \\ 0 \end{bmatrix} \Delta \varphi_\delta + \begin{bmatrix} 2\zeta_d\omega_d k_d k_{ppll}/U_{pd0} \\ 0 \end{bmatrix} \Delta u_{pq} \end{aligned} \quad (18)$$

and the output vector

$$\Delta y_d^c = \Delta \gamma_1. \quad (19)$$

The new state variables are added to the uncompensated system (14), to realize the small-signal state-space model of the compensated system as

$$[\Delta \dot{x}_{\text{comp}}] = [A_{\text{comp}}][\Delta x_{\text{comp}}] \quad (20)$$

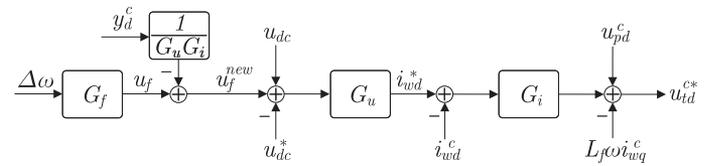


Fig. 6. Model of the d -axis controller.

in which

$$\Delta x_{\text{comp}} = [\Delta x_{\text{uncomp}} \quad \Delta \gamma_1 \quad \Delta \gamma_2]_{1 \times 15}^T$$

and the corresponding state matrix is provided in Appendix A.

It is noteworthy that the proposed compensator can be also interpreted as modifying $G_f(s)$ into a new transfer function named $G_f^{\text{new}}(s)$, which is obtained as follows. Consider the d -channel of controller in Fig. 4. Moving the signal $y_d^c(s)$ ahead of the inner current and outer voltage controllers results in Fig. 6. Hence, the new ancillary voltage signal $u_f^{\text{new}}(s)$ is derived from

$$u_f^{\text{new}}(s) = \underbrace{G_f(s)}_{u_f(s)} \Delta \omega - \frac{y_d^c(s)}{G_u(s)G_i(s)}. \quad (21)$$

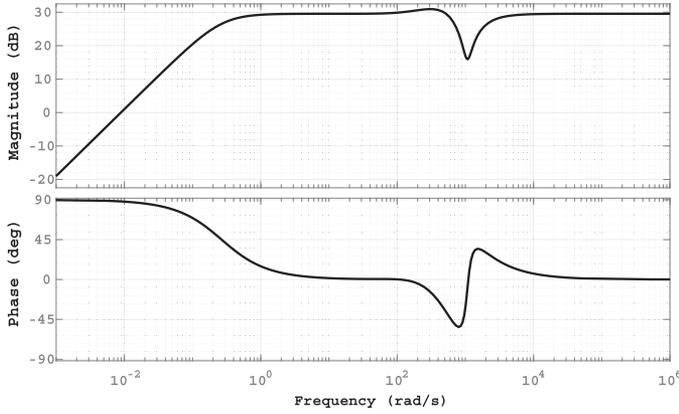


Fig. 7. Frequency response of $G_f^{\text{new}}(s)$.

Substituting (17) into (21) gives

$$u_f^{\text{new}}(s) = \underbrace{\left(G_f(s) - \frac{G_c(s)}{G_u(s)G_i(s)} \right)}_{G_f^{\text{new}}(s)} \Delta\omega. \quad (22)$$

Fig. 7 illustrates the frequency response of $G_f^{\text{new}}(s)$ when the control parameters are set according to Table I. As observed from this figure, $G_f^{\text{new}}(s)$ manipulates the DVI gain as a function of frequency. Assume a grid frequency disturbance arises. The grid frequency falls (or rises), which includes HF components (consider HF section of Fig. 7). Then, the amplitude of $G_f^{\text{new}}(s)$ is 29.55 dB (30 V s)—just equal to k . However, it reduces to 15.9 dB (6.2 V s) at the frequency about 1035 rad/s to hold the converter controller stable [see mode 4 in Fig. 8(b)]. As the grid frequency reaches recovery and quasi-steady sections (moving toward low- and zero-frequency components, respectively), $G_f^{\text{new}}(s)$, and thus $u_f^{\text{new}}(s)$, starts converging to zero so as the dc-link voltage can regain its nominal value.

B. Design Process

Three parameters k_d , ζ_d , and ω_d are precisely designed aiming to eliminate adverse impact of the DVI technique on the converter stability. We consider the worst-case scenario, i.e., SCR=2 and $k=30$, in the design process [cf. Fig. 5(e)]. Remarkably, mode 8 in Fig. 8 corresponds to the employed compensator (17).

First, assume the damping ratio is $\zeta_d = 0.6$. Fig. 8(a) demonstrates the impact of compensator gain and cut-off frequency on the system eigenvalues when k_d varies between $0 \leq k_d \leq 3.2$ Vs and ω_d takes two values, 600 and 800 rad/s. Explicitly, increasing the gain k_d yields movement of unstable mode 4 toward the left-hand side of complex s-plane. This trend occurs in a faster rate for higher values of cut-off frequency. Thus far, the parameters k_d and ω_d are selected 3.2 Vs and 800 rad/s, respectively. Fig. 8(b) depicts the eigenvalue loci of the conversion system when ζ_d rises to 0.8 (only eigenvalues with positive imaginary parts are displayed for good visibility). As per this figure, $\zeta_d = 0.8$ leads to a more damped system. Herein, we consider $\zeta_d = 0.8$. Hence, it is concluded that the ancillary compensator 1) does not affect

the dominant poles (i.e., modes 1, 2, and 3), 2) completely damps mode 7 as k_d increases, and 3) it relocates the unstable mode 4 from $223 \pm j1135$ to the stable point $-72 \pm j1035$ [cf. Figs. 5(e) and 8(c)]. This signifies that the negative impact of the DVI function (aimed at transient grid frequency enhancement) is eliminated by proper design of (17).

VI. VALIDATIONS

To verify the results provided in preceding sections, a time-domain model of the system illustrated in Fig. 1 is built in MATLAB. The power rating and operating voltage of the converter are 20 kVA and 400 V, respectively. We assume that the permissible fluctuation range for dc-side voltage is 10%, i.e., 75 V. Other parameters of the design are summarized in Table I. Simulations are divided into two case studies, 1) the ancillary compensator is canceled out to support the instability problem discussed in Section IV, and 2) (17) is considered to show the efficacy of compensation technique.

A. Case I

In this subsection, the compensator (17) is deactivated and the DVI gain is set to 30 Vs. Fig. 9 depicts the output-controlled variables p_{out} , q_{out} , and u_{dc} in normal grid condition, i.e., no frequency disturbance. The active and reactive power set points change at $t = 1$ and 2 s by -25% and $+100\%$, respectively. From Fig. 9(a)–(c), it is observed that the system operates stable and the variables reach their nominal values after a transient. As indicated earlier in Section IV, but the converter subjects to instability when a frequency perturbation occurs in the grid. This is justified by the fact that the DVI gain shifts a local mode associated with the control system toward the right-hand side of s-plane if any frequency oscillation arises. To indicate this issue, a grid frequency disturbance is considered at $t = 2$ s and the results are presented in Fig. 10. As can be seen, the controlled variables follow the references; however, the converter becomes unstable after the defined disturbance. The results agree with the eigenvalue analysis provided in Fig. 5(e).

B. Case II

Here, the ancillary compensator is added to the controller to solve the instability issue raised by the DVI loop. Two cascading grid frequency disturbance (with the same amplitude) occur at $t = 2$ and 4 s. Fig. 11 illustrates the controlled variables p_{out} , q_{out} , and u_{dc} . As observed from Fig. 11(a), the output active power reaches from 20 to 21.8 kW (23.4 kW) following the first (second) perturbation. The supplementary power is provided by discharging the dc capacitance, which is analogous with the released kinetic energy of real SGs to regain the power balance during transient. The reactive power response of the converter is shown in Fig. 11(b). It peaks at -0.8 and -1.6 kVar during the first and second transients, respectively. Then, it drops to the set point of 0 after 1 s. The dc-side voltage oscillations in case of applying conventional and modified DVI functions are presented in Fig. 11(c). With conventional DVI loop, the dc voltage drifts to lower value in each disturbance and it is not

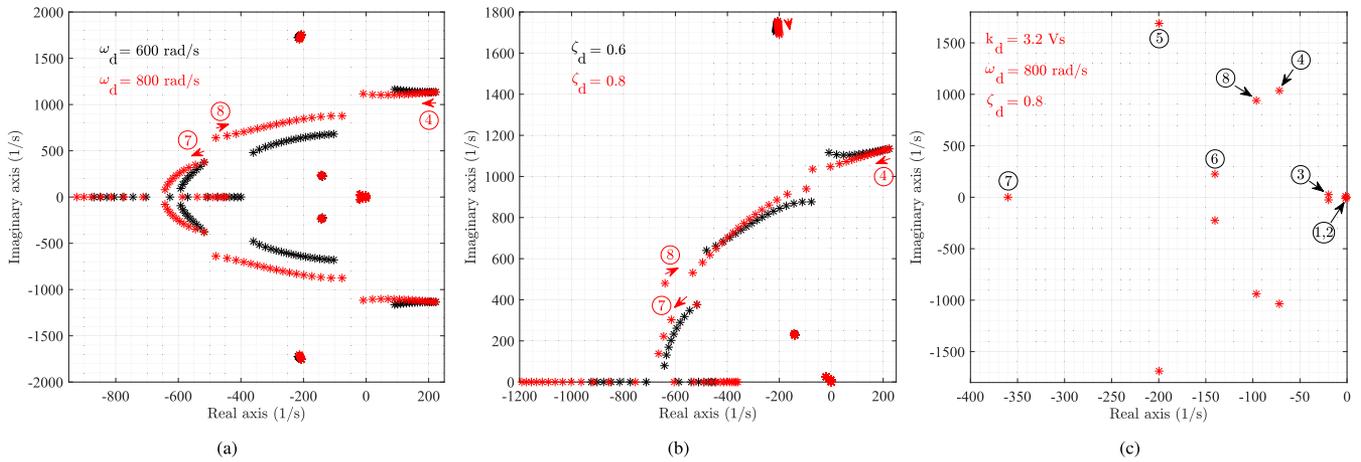


Fig. 8. Effect of (a) ω_d , (b) ζ_d on the converter dynamics, and (c) final pole diagram of the compensated system.

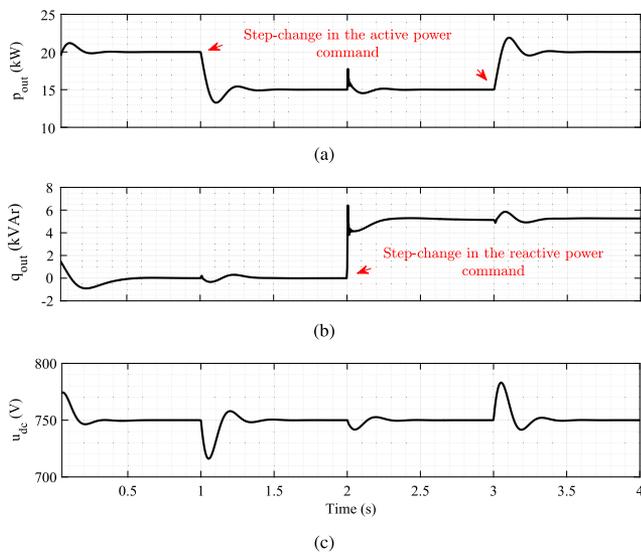


Fig. 9. Converter outputs (remark: the grid operates normally).

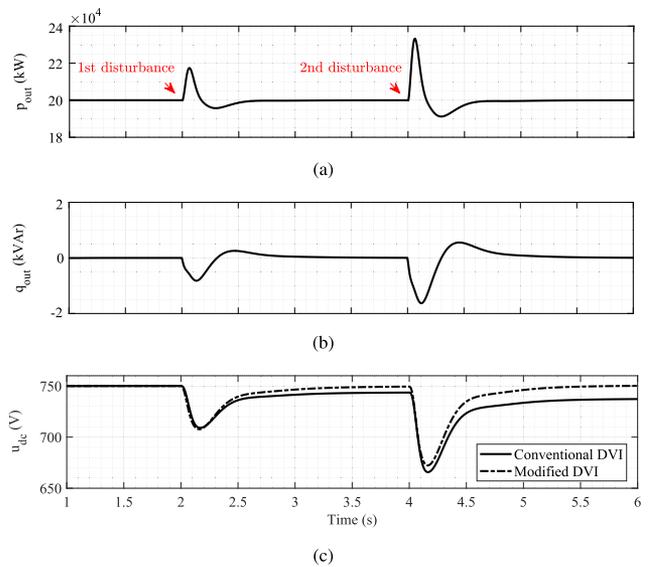


Fig. 11. Compensated converter outputs (remark: cascading frequency perturbations arise at $t = 2$ s and $t = 4$ s).

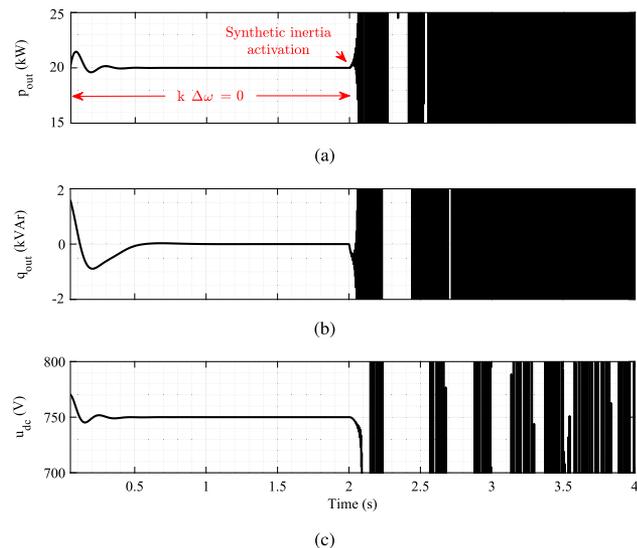


Fig. 10. Uncompensated converter outputs (remark: grid frequency perturbation arises at $t = 2$ s).

reverted to the reference of 750 V. Remarkably, the higher $\Delta\omega$ is, the more dc voltage drops (i.e., $\Delta u_{dc} = k\Delta\omega$ holds true). This problem is addressed by employing the modified DVI function expressed in (3). From Fig. 11(c), it is observed that the dc-bus voltage drops to 710 V (675 V) and recovers to its nominal value after the first (second) disturbance. The diminution of capacitor voltage indicates that the discharged energy supports the grid frequency, resulting in better transient frequency regulation. It is noteworthy that the dc voltage is within the acceptable range.

The frequency oscillations measured by the PLL at the PoI are depicted in Fig. 12. When the converter is equipped with the DVI loop, the grid experiences lower frequency nadir and the RoCoF level is enhanced by 23% collated with the case in which the DVI function staying nullified. It is worth pointing out that both conventional and modified DVI methods lead to the same frequency stability metrics. The difference is the dc-side voltage restoration capability of the modified DVI technique.

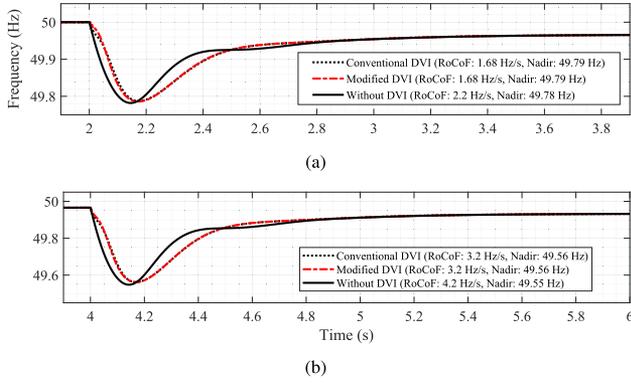


Fig. 12. Frequency excursion measured by the PLL at the PoL. (a) First disturbance. (b) Second disturbance.

Hence, as per Figs. 11 and 12, we can conclude that the compensator (17) holds the converter augmented with the DVI technique stable in weak grid conditions. Moreover, (3) restores the dc-side voltage to its reference in spite of grid frequency deviation after the disturbance.

VII. CONCLUSION

Herein, an enhanced DVI-based control strategy for grid-tied power converters employed in weak power systems has been proposed. As stated in Sections II and IV, the conversion system

augmented with the conventional DVI method has two drawbacks: 1) the dc-side capacitor voltage is not restored to its nominal value unless the grid power balance holds true, and 2) the DVI gain induces instability to the converter operating in weak grids. The higher DVI gain, the better transient frequency stability after disturbance; however, it deteriorates the converter stability. The two aforesaid problems have been addressed by 1) modifying the DVI function so as not to affect the outer loop voltage regulator after transient, and 2) applying an ancillary compensator, which eliminates the adverse impact of the DVI gain on the system stability. Hence, the converter operates stable in weak grids whilst providing maximum synthetic inertia support. The efficacy of the control framework has been depicted via simulations. The results illustrated that the grid frequency rate of change following a disturbance has improved by 23% in comparison to the case in which the DVI loop staying nullified. As an interesting topic for future work, the proposed controller could be applied to grid-interactive MMCs in power systems with high shares of RESs integrating through MMCs. This proposal could provide more synthetic inertia coefficient (and thus better grid frequency support) as larger capacitance is available in the dc-side of MMCs.

APPENDIX A

STATE AND INPUT MATRICES

The state and input matrices corresponding to the uncompensated and compensated systems are provided in this Appendix,

$$\begin{aligned}
 A_{\text{uncomp}} = & \begin{bmatrix} -k_{ppll} & 1 & 0 & 0 & 0 & \frac{k_{ppll}}{U_{pd0}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -k_{ipll} & 0 & 0 & 0 & 0 & \frac{k_{ipll}}{U_{pd0}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ a_{3,1} & \frac{-kk_{pu}k_{pi}}{L_f} & \frac{-k_{pi}-R_f}{L_f} & 0 & 0 & \frac{-kk_{pu}k_{pi}k_{ppll}}{L_f U_{pd0}} & \frac{k_{pi}k_{pu}}{L_f} & \frac{k_{pi}}{L_f} & \frac{1}{L_f} & 0 & 0 & 0 & \frac{-k_{pi}k_{pu}k_{pf}}{L_f} \\ a_{4,1} & 2I_{wd0} & 2\omega_0 & \frac{-k_{pi}+R_f}{L_f} & 0 & \frac{2k_{ppll}I_{wd0}}{U_{pd0}} & 0 & 0 & 0 & \frac{1}{L_f} & 0 & 0 & 0 \\ -k_{ppll}U_{pq0} & U_{pq0} & \frac{1}{C_f} & 0 & 0 & \frac{k_{ppll}U_{pq0}}{U_{pd0}} + \omega_0 & 0 & 0 & 0 & 0 & \frac{-1}{C_f} & 0 & 0 \\ k_{ppll}U_{pd0} & -U_{pd0} & 0 & \frac{1}{C_f} & -\omega_0 & -k_{ppll} & 0 & 0 & 0 & 0 & 0 & \frac{-1}{C_f} & 0 \\ 0 & 0 & a_{7,3} & a_{7,4} & a_{7,5} & a_{7,6} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ kk_{iu}k_{ppll} & -kk_{iu} & 0 & 0 & 0 & \frac{-kk_{iu}k_{ppll}}{U_{pd0}} & k_{iu} & 0 & 0 & 0 & 0 & 0 & -k_{iu}k_{pf} \\ a_{9,1} & -kk_{pu}k_{ii} & -k_{ii} & 0 & 0 & \frac{-kk_{pu}k_{ii}k_{ppll}}{U_{pd0}} & k_{ii}k_{pu} & k_{ii} & 0 & 0 & 0 & 0 & -k_{ii}k_{pu}k_{pf} \\ k_{ii}I_{wd0} & 0 & 0 & -k_{ii} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -k_{ppll}I_{q0} & I_{q0} & 0 & 0 & \frac{1}{L_g} & \frac{k_{ppll}I_{q0}}{U_{pd0}} & 0 & 0 & 0 & 0 & \frac{-R_g}{L_g} & \omega_0 & 0 \\ k_{ppll}I_{d0} & -I_{d0} & 0 & 0 & 0 & \frac{1}{L_g} - \frac{k_{ppll}I_{d0}}{U_{pd0}} & 0 & 0 & 0 & 0 & -\omega_0 & \frac{-R_g}{L_g} & 0 \\ \frac{kk_{ppll}}{C_{dc}u_{dc}^*} & \frac{-k}{C_{dc}u_{dc}^*} & 0 & 0 & 0 & \frac{-kk_{ppll}}{C_{dc}u_{dc}^*U_{pd0}} & 0 & 0 & 0 & 0 & 0 & 0 & \frac{-k_{pf}}{C_{dc}u_{dc}^*} \end{bmatrix}_{13 \times 13} \\
 B_{\text{uncomp}} = & \left(0_{2 \times 2} \begin{pmatrix} \frac{2k_{pi}}{3L_f U_{pd0}} & 0 \\ 0 & \frac{k_{pi}}{L_f} \end{pmatrix} 0_{2 \times 2} \begin{pmatrix} \frac{1}{C_{dc}u_{dc}^*} & 0 \\ 0 & 0 \end{pmatrix} \begin{pmatrix} \frac{2k_{ii}}{3U_{pd0}} & 0 \\ 0 & k_{ii} \end{pmatrix} 0_{3 \times 2} \right)_{2 \times 13}^T \\
 A_{\text{comp}} = & \begin{pmatrix} & & & & & & & & & & & 0_{2 \times 2} \\ & & & & & & & & & & & \begin{pmatrix} \frac{1}{L_f} & 0 \end{pmatrix} \\ & & & & & & & & & & & 0_{10 \times 2} \\ \begin{pmatrix} -2\zeta_d \omega_d k_d k_{ppll} & 2\zeta_d \omega_d k_d \\ 0 & 0 \end{pmatrix} & & 0_{2 \times 3} & & \begin{pmatrix} \frac{2\zeta_d \omega_d k_d k_{ppll}}{U_{pd0}} \\ 0 \end{pmatrix} & & 0_{2 \times 6} & & \begin{pmatrix} -2\zeta_d \omega_d & 1 \\ -\omega_d^2 & 0 \end{pmatrix} \end{pmatrix}_{15 \times 15}
 \end{aligned}$$

where

$$a_{3,1} = \frac{k k_{pu} k_{pi} k_{ppll} - k_{pi} I_{wq0} + U_{pq0} - U_{tq0}}{L_f} + I_{wq0} k_{ppll}$$

$$+ \omega_0 I_{wd0} - k_{ppll} I_{wq0}$$

$$a_{4,1} = \frac{k_{pi} I_{wd0} - U_{pd0} + U_{td0}}{L_f} + \omega_0 I_{wq0} - k_{ppll} I_{wd0}$$

$$- k_{ppll} I_{wd0}$$

$$a_{7,3} = \frac{-3U_{pd0}}{2C_{dc}u_{dc}^*}$$

$$a_{7,4} = \frac{-3U_{pq0}}{2C_{dc}u_{dc}^*}$$

$$a_{7,5} = \frac{-3I_{wd0}}{2C_{dc}u_{dc}^*}$$

$$a_{7,6} = \frac{-3I_{wq0}}{2C_{dc}u_{dc}^*}$$

$$a_{9,1} = k k_{pu} k_{ii} k_{ppll} - k_{ii} I_{wq0}.$$

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