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A 0.9-Nyquist-Band Digital Timing Mismatch Correction for Time-Interleaved ADCs Achieving Delay Tuning Range of 0.12-Sample-Period

Ilia Kempi, Okko Järvinen, Marko Kosunen, *Member, IEEE,* Vishnu Unnikrishnan, *Member, IEEE,*
Kari Stadius, *Member, IEEE,* and Jussi Ryynänen, *Senior Member, IEEE*
Department of Electronics and Nanoengineering, Aalto University, Espoo, Finland
Email: ilia.kempi@aalto.fi

***Abstract*—Time-interleaved analog-to-digital converters (TI-ADC) require channel matching in terms of offset, gain, and sampling clock skew to achieve best data conversion performance. Conventionally, correction of skew mismatch is realized with analog delay lines, making it challenging for high-speed ADC designs to achieve fine delay resolution over wide tuning range while maintaining low clock jitter. Digital skew correction allows greater flexibility than analog solutions, but is hindered by a significant hardware footprint. This paper demonstrates digital filter-based timing skew correction approach suitable for on-chip implementation. In a 10-bit 8-channel TI-ADC the proposed structure corrects mismatch magnitudes up to 0.12 sample period across 0.9 Nyquist band while requiring only 65% hardware of similar architectures of equivalent performance. The presented digital circuit uses reduced combinational paths and operates at a clock rate of single ADC channel, making it applicable for digitally-assisted high-speed TI-ADCs.**

I. Introduction

Time-interleaving (TI) is a widely adopted analog-to-digital converter (ADC) technique which enables fast sample rates while maintaining high resolution. With current nanometer-scale process nodes which favor digital-intensive designs, recent TI-ADC implementations tend to offload the fine-tuning of channel calibration into the digital domain. This is especially popular solution for gain and offset mismatches, as for both of these errors the estimation and correction can be mostly confined within individual channel data path and realized with simple digital arithmetics [1], [2].

Matching of the clock skew is more complex, as it requires collecting extra information from all TI channels to estimate the sampling time error. Various techniques have been reported for carrying out skew estimation on-chip, either by employing auxiliary analog circuits [3]–[5] or applying statistical methods in the digital domain to a sampled signal of known properties [6]–[10]. For correcting the skew mismatch, the most popular approach by far is to directly tune the phase of the sampling clocks in the analog domain with delay lines [4], [7], [11]. Implementation of analog delay elements in clock path introduces design challenges in terms of component matching, delay monotonicity, jitter, as well as trade-off between delay resolution and delay range [12], [13]. The analog issues are further magnified in high-speed designs, where absolute clock skew translates into larger time error relative to the sampling period T_s. This is especially a concern in highly parallelized TI-ADC, where residual mismatch imposes a performance limit, e.g. to achieve 9-bit resolution with 4-channel converter, skew deviation must not exceed $8 \cdot 10^{-4}\ T_s$ [14], [15]. By performing skew correction in the digital domain, the residual timing error can be arbitrarily minimized, relaxing the analog constraints for TI clock distribution. If the skew mismatch is known, it is possible to shift the sampling instants of digitized time series with linear interpolation. However, with this technique the compensation range is limited to about 0.06 T_s [5], [16]. On the other hand, digital reconstruction filters offer better skew tuning range and delay resolution but require a trade-off between hardware cost and usable bandwidth. Hence, it is usually implemented off-chip [17], [18].

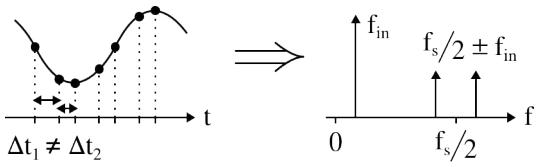

Fig. 1. Effect of timing mismatch in a 2-channel TI-ADC.

This work examines a combination of design optimizations for efficient digital skew mismatch correction, enabling delay tuning ranges up to 0.12 T_s at 10-bit ADC resolution while retaining a wide usable bandwidth and operating at a clock rate of a single TI channel. The proposed digital structure is suitable for on-chip implementation in highly parallelized high-speed TI-ADCs, facilitating scalable converter designs aiming for fully digital mismatch compensation.

This paper is structured as follows, Section II introduces the timing error model, Section III presents the error correcting algorithm, and Section IV describes relevant hardware optimizations followed by performance overview. Section V summarizes and concludes the paper.

II. Effect of Skew Mismatch in TI-ADC

Systematic sampling time error in M-channel TI-ADC manifests at the interleaved output as a periodic signal with characteristic spectral footprint [19], as illustrated in Fig. 1.

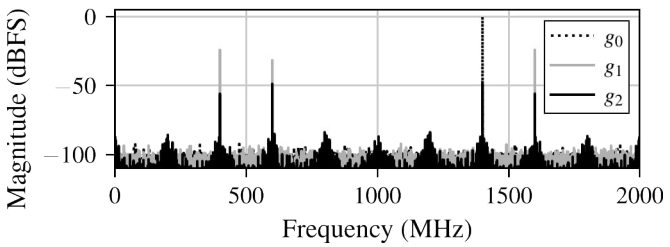

Fig. 2. Spectrum of Taylor expansion terms g of a sampled 1.4 GHz sinusoid with 10-bit 4 GS/s 4-channel TI-ADC with clock mismatch of channels 2,3, and 4 being 17, -6, and -11 ps.

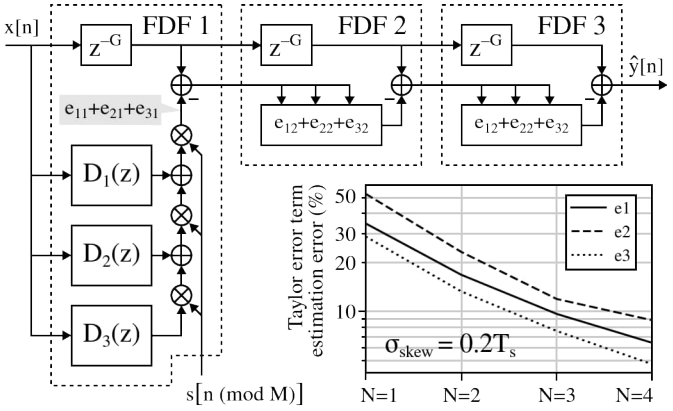

Fig. 3. FDF chain for skew compensation. Each consecutive stage provides better error term estimation.

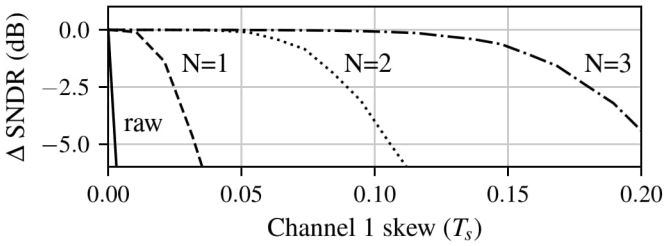

Fig. 4. Retention of SNDR against increasing skew mismatch using N FDF stages in 10-bit 8-channel TI-ADC sampling a 770 MHz input signal at a rate of 2 GHz. The timing skew mismatch is isolated to ADC channel 1 and the rest of the channels are not skewed.

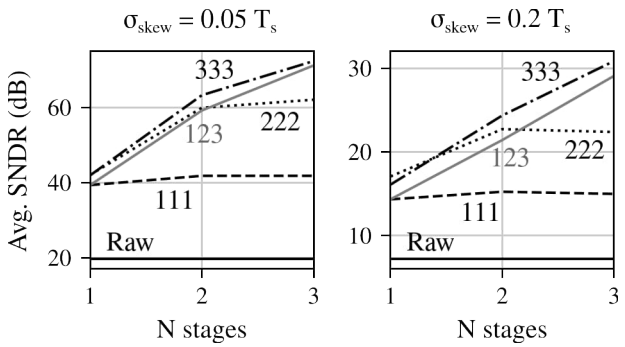

Fig. 5. Performance of different filter chain configurations in presence of normally distributed skew mismatch of deviation 0.05 T_s (left) and 0.2 T_s (right). Each point is an average of 100 trials with ideal 12-bit 8-channel TI-ADC sampling 770 MHz input signal at a rate of 2 GHz.

For purposes of error correction, the error signal can be approximated in the time domain with Taylor expansion of a continuous input signal $x(t)$ at ideal (non-skewed, uniformly spaced) sampling points. For each TI channel m, corresponding Taylor series terms g_m of order l are expressed as

$$g_{m,l}[n] = x^{(l)}\big((nM+m)T_s\big)\frac{(\Delta t_m)^l}{l!}, \qquad (1)$$

where Δt_m is the relative skew mismatch of corresponding TI channel out of M total channels [20]. The sampled signal $x[n]$ then consists of M interleaved terms $g_{m,0}[n]$, which constitute uniformly sampled original signal $y[n]$ and a uniformly sampled error signal $r[n]$ containing $\sum_{l=1}^{\infty} g_{m,l}[n]$ interleaved error terms. In Fig. 2, the spectrum of $y[n]$ equivalent to g_0 is overlaid with the first two error terms g_1 and g_2 that are characterized by pronounced spurious tones [19]. In practice $\Delta t_m << T_s$, so the higher-order terms (e.g. $l > 4$) of (1) are negligible unless Δt_m is exceptionally large and the l-th derivative of x is significant, which is expected at high f_{in}.

III. Error Correction Method

To estimate the Taylor series of $x(t)$, an array of filters is applied with frequency responses $D_l(j\omega)$ approximating that of an ideal l-order differentiator $(j\omega)^l$. This array forms a time-varying fractional delay filter (FDF), also known as a Farrow structure [21]. Each sub-filter branch is weighted with a periodic sequence of time delay factor estimates $s[m] = \Delta\hat{t}_m$ for each channel $m = n \pmod M$ as shown in Fig. 3. In this manner, each branch realizes the computation of the first three error terms $e_l = g_l$ as described by (1), with the bypass term g_0 implemented as z^{-G} in order to equalize for the group delay G of $D_l(z)$.

A major drawback of the FDF approach is the use of the non-uniformly sampled signal $x[n]$ in approximating the derivative of $x(t)$, which limits the accuracy of the calculated error signals e_l. To improve the derivative estimation, a chain of N FDF stages is introduced as shown in Fig. 3, effectively reducing e_l inaccuracy in each consequent stage. Fig. 4 demonstrates how multiple FDF stages can maintain the SNDR of an interleaved ADC output in controlled skew mismatch conditions.

Utilization of long FDF chains for on-chip skew correction requires significant digital resources. One option is to limit the correction range and utilize only one-stage first-order term compensation as reported in [1], [2], [18], which is sufficient for TI-ADCs where the accounted relative skew mismatch is not significant. Alternatively, the number of error terms in individual FDF elements within the chain can be reduced. Fig. 5 shows SNDR simulations of skew compensation by different FDF chain configurations of up to three stages. The configurations are enumerated with sequences that denote number of error terms used for each successive FDF in the chain. The simulation results in Fig. 5 indicate that reducing

the number of error terms limits the performance of the later stages, whereas using more error terms than the effective length N of the chain yields no significant benefit. Notably, configuration "123", which uses exactly n terms at n-th stage, exhibits the same compensation performance as configuration "333" with maximum amount of terms, which aligns with analysis provided in [20], [21]. In the following sections, only the configuration "123" will be considered, as it provides up to 0.12 T_s skew correction range without loss of SNDR and requires only $2/3$ of the most effective $N \times N$ FDF chain configuration.

IV. Digital Implementation

This section highlights the practicalities of realizing the introduced FDF chain using finite impulse response (FIR) filters. Since the order of an FIR structure largely defines its implementation cost in terms of registers, adders, and fixed multipliers, the filter order K will be considered as the main cost metric along with the number of unique multipliers A.

A. Filter Design

Two alternatives exist for designing wideband differentiators, one method focuses on coefficient optimization based on frequency response specification [22], [23], other method considers generating time-domain sequences directly with coefficients given by polynomials [24], [25]. The latter approach is utilized in this work for its computational simplicity and sufficient transfer characteristics to realize skew mismatch correction.

The impulse response of the first-order differentiator

$$d_1(n) = \frac{1}{2\pi}\int_{-\pi}^{\pi} j\omega e^{j\omega n} d\omega = \begin{cases} 0, & n = 0 \\ \frac{-1^n}{n}, & n \neq 0 \end{cases} \quad (2)$$

is realizable as a Type-III linear-phase FIR filter [24] of order K with a uniform group delay of $K/2$. For purposes of skew mismatch correction, only even K are considered to achieve integer group delay. The sequence is then multiplied by a windowing function in order to reduce the characteristic ringing in the frequency domain that is typical to finite $d_1(n)$. Sequences $d_l(n)$ of higher orders l can be obtained by repeated convolution of $d_1(n)$ with itself to achieve an approximation of $D_l(j\omega) = (j\omega)^l$. Each additional convolution increases the length of $d_l(n)$. To equalize the group delay of the resulting filter bank, each obtained sequence is truncated to match a $(K+1)$-long window function centered at the midpoint $d_l(K/2)$. Compared to the frequency-domain design approach, higher order ($l \geq 2$) differentiator sequences obtained with this method exhibit increasingly larger deviation from the ideal $(j\omega)^l$, but are still reasonably effective for purposes of skew correction as is demonstrated in the following sections.

B. Efficient High-Throughput Filtering

In the context of high-speed TI-ADC, filtering the interleaved signal is infeasible, and thus polyphase filters may be applied directly to the parallel TI channel data [18], [22]. To achieve wide compensation bandwidths it is imperative to use high-order $D(z)$, which in turn requires adder trees of width at least $K/2$ in direct FIR implementation, which may be challenging to achieve in high-speed designs. We suggest to use a polyphase version of the transposed FIR structure, which allows to restrict adder tree width to number of TI channels M. Fig. 6 shows an example transposed polyphase FIR filter of 4th order. With polyphase input $x_m[n] = x[Mn+m]$, the computation of output Y for each output channel p is

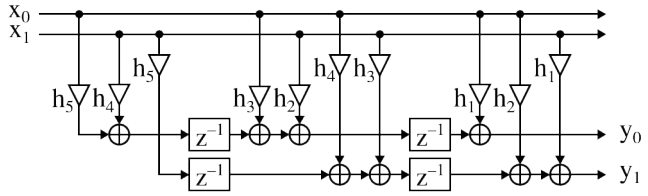

Fig. 6. Transposed polyphase structure implementing a 4th order FIR filter in a 2-channel double rate system.

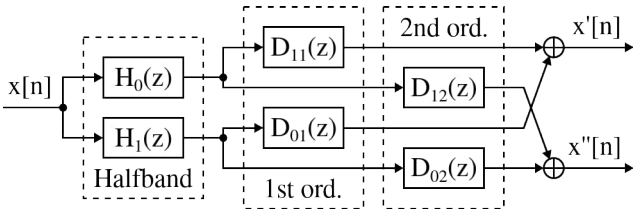

Fig. 7. Multirate differentiator bank for second FDF stage. $H_0(z)$, $D_{0\mathrm{X}}(z)$ and $H_1(z)$, $D_{1\mathrm{X}}(z)$ correspond to even and odd polyphase components of respective filters.

$$Y_p(z) = \sum_{m=0}^{M-1} X_m(z) H_{m-p \pmod M}(z) z^{-\lceil \frac{-p+m}{M} \rceil}, \quad (3)$$

where $H_k(z)$ is a k-th polyphase component of the FIR impulse response. To align the group delays of each filter branch to the same delay cycle, order of $H(z)$ must be divisible by $2M$. Upon expanding (3), we can see that in order to obtain all outputs $Y_p(z)$, each of the M interleaved input components $X_m(z)$ must be combined with every polyphase component of $H(z)$, but not necessarily within one p computation datapath as in direct-form polyphase FIR implementations. This observation suggests that linear-phase FIR filters realized in this fashion can be optimized for symmetrical multipliers, similarly to their direct-form counterparts [24].

C. Hardware Cost Optimizations

The bandwidth of the FDF depends on the aggregate bandwidths of filters $D_l(z)$, which are set by filter order K. This dependency translates to a design trade-off, where adding hardware (multipliers) increases the usable skew correction bandwidth with diminishing returns. By accounting for symmetry of $d_l(n)$ and the fact that for $d_{l=1,3}(K/2) = 0$, total multiplier count for "123" FDF chain configuration is

$$A_{123} = 6 \cdot (K/2) - 4. \quad (4)$$

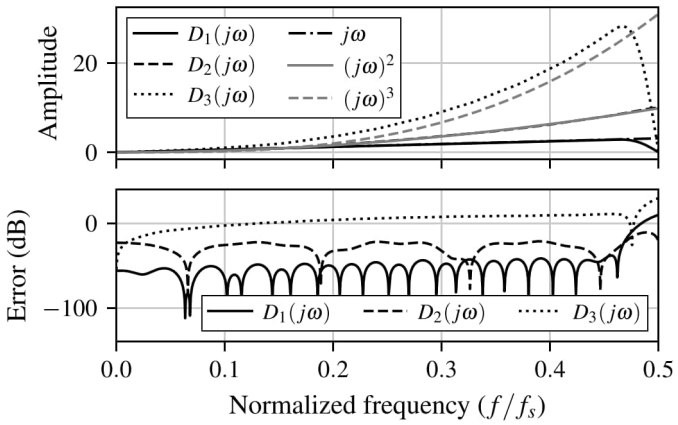

Fig. 8. Accuracy of multirate differentiator realization with FIR filters of order $J = 14$ and half-band filer of order $B = 92$.

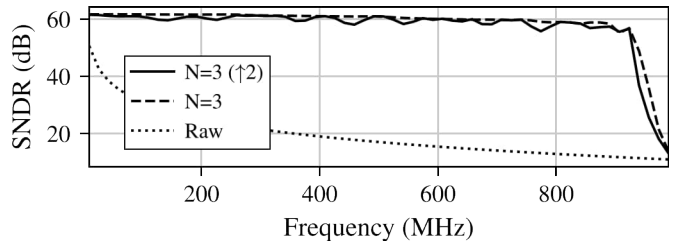

Fig. 9. Simulation of direct ($N = 3$, $K = 64$) and multirate implementations ($N = 3$, $B = 88$, $J = 14$) of FDF chain used for skew correction in a 2 GHz 10-bit 8-channel TI-ADC. Timing skew mismatch applied to channels 2–8 is -50, -40, 55, 45, 60, 40, and -35 ps.

To improve hardware cost efficiency, we employ band-limiting, up-sampling, and polyphase decomposition as described in [23], [26]. Combination of these multi-rate techniques is further referred to as $(\uparrow 2)$ in notation. Fig. 7 gives an example of an optimized FDF implementation, where an additional halfband filter $H(z)$ is utilized to reduce the order J of consequent filters $D_l(z)$. The combined bandwidth of the multirate filter bank then depends on the order B of the half-band filter [23]. Fig. 8 shows the multirate differentiator bandwidth achievable with only $J = 14$ by using half-band of order $K = 92$, which is approximately equivalent to a direct implementation of individual differentiators with $K = 65$. Regardless of significant mismatch with ideal differentiator response, multirate filter banks perform as well as its direct implementation, as shown in Fig. 9. In both cases, SNDR of the corrected signal rapidly degrades past frequency at which the differentiator approximations diverge from the ideal $(j\omega)^l$ shape. In the FDF chain, the multirate optimization is applicable to stages 2 and 3 only, where multiple differentiators may benefit from simultaneous length reduction. Considering symmetrical $D(z)$ and $H(z)$, the total multiplier count of the optimized structure is

$$A_{123(\uparrow 2)} = \underbrace{K/2-1}_{D(z)\text{ of }N=1} + \underbrace{2\cdot(B/2)}_{H(z)\text{ of }N=2,3} + \underbrace{5\cdot(J/2)-3}_{D(z)\text{ of }N=2,3}. \quad (5)$$

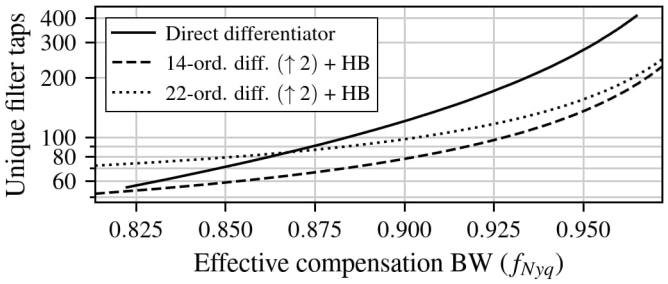

Fig. 10. Comparison of $N = 3$ FDF chain implementation cost for direct and multirate filter bank implementations to achieve a set compensation BW.

TABLE I
COMPARISON OF IMPLEMENTATION COST AND PERFORMANCE

Implementation	Multipliers for BW[a] (f_{Nyq})			Δt_{max}[b]
	0.8	0.9	0.95	(T_s)
N=1 Direct [1], [2], [18]	8	20	46	0.01
N=3 Direct [17], [20], [21]	50	122	278	0.12
N=3 Multirate	52	79	136	0.12

[a] Per single channel. Example filters used for profiling are designed in the time domain as described in section IV-A
[b] With test mismatch isolated to one channel (see Fig. 4)

In the new cost breakdown, in addition to parameter K, the bandwidth-sensitive portion is also defined by $H(z)$ order B, while $D(z)$ component becomes a static overhead. Fig. 10 demonstrates the bandwidth-to-cost improvement between (4) and (5) past 0.825 of Nyquist frequency f_{Nyq}. Note that using a multirate filter bank with elements $D(z)$ of order 22 uniformly increases the hardware cost overhead when compared to $D(z)$ of order 14, confirming that $H(z)$ dictates the usable bandwidth of the multirate structure. Table I enumerates the multiplier cost requirements of different skew correction schemes for different bandwidth specifications. The presented digital structure employs both the multi-stage compensation scheme [20], [21] and the multirate FDF optimizations [23], [26] to achieve state-of-the-art skew correction performance while providing significant hardware savings at compensation bandwidths of 0.9 f_{Nyq} and beyond.

V. CONCLUSION

This work demonstrates how FDF-based timing correction approach scales in terms of usable bandwidth as well as in terms of tolerable timing skew range. We suggest several structural optimizations for wide-bandwidth, wide-range, and high speed algorithm implementation. Test case of 10-bit 8-channel TI-ADC shows that the optimized reconstruction structure tolerates mismatch magnitudes up to 0.12 Ts, and requires only 79 fixed multipliers per channel to cover 0.9 of Nyquist bandwidth. The presented algorithm makes efficient use of digital hardware and is suitable for on-chip implementation along with the TI-ADC. By allowing extensive skew correction in the digital domain, the proposed architecture adds flexibility and enables wider trade-offs in terms of analog design.

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