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A 2 GS/s 9-bit Time-Interleaved SAR ADC with Overlapping Conversion Steps

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Abstract—This paper presents a wideband 8-way time-interleaved (TI) 9-bit successive approximation register (SAR) analog-to-digital converter (ADC) with overlapping conversion steps that improve the speed of operation. The ADC generates its clocks using a synchronous counter based circuit which reduces the SAR delay. A common-mode reference based split capacitor array digital-to-analog converter (DAC) is implemented that achieves high speed and low power consumption. Simulation results are presented for the ADC designed in a 22 nm CMOS process. The TI ADC achieves at least 7.7 ENOB at 2 GS/s and consumes a total of 19.8 mW from 0.8 V supplies, resulting in 47.6 fF/conv-step. The single ADC achieves 8.34 ENOB at 250 MS/s, consuming 1.43 mW in total and 17.7 fF/conv-step.

Index Terms—SAR ADC, time-interleaved ADC, high-speed ADC

I. INTRODUCTION

New 5G and upcoming 6G cellular communication standards specify highly ambitious data throughput among other improved metrics and thus impose stricter requirements for wireless array transmitters and receivers. A commonly recognized bottleneck in receiver systems is the maximum sample rate of the ADC which limits the conversion bandwidth. Modern systems require ADCs with a large bandwidth and low power consumption while maintaining a moderately high resolution, and future receivers tighten the requirements further [1]. High-speed ADCs are required also in wireline communications in addition to wireless.

Applications requiring low power and moderate resolution typically do the conversion using SAR ADCs, however their maximum sample rate is usually limited comparing to other architectures. Time-interleaving is a technique where several converters are used in different phases to multiply the total sample rate. SAR ADCs are ideal for time-interleaving due to their small area and power consumption that result in manageable total area and power when using multiple parallel converters. Statistics show that TI SAR ADCs typically achieve better overall performance than other alternatives [2]. In addition to time-interleaving, there have been several successful attempts to improve the speed of the single SAR ADC to obtain a further increase in bandwidth. Common ideas for increasing the sample rate are enhancing the SAR speed [3], using a faster sub-ADC to solve some bits [4] or using asynchronous logic to minimize conversion time [5].

This paper presents an 8-way time-interleaved 2 GS/s 9-bit SAR ADC design that overlaps conversion steps to improve the maximum operating speed. The sample rate is increased by solving each bit over two clock cycles, which reduces the subcircuit delay requirements. Overlapping is used to fit all bit decisions to the short conversion window. In addition to reducing the delay requirements, our design improves the SAR delay over the conventional asynchronous structure by using synchronous operation. The capacitive DAC (CDAC) speed is maximized and power minimized by reducing the number of unit capacitors and using an additional control voltage. The converter is targeted for modern true-time-delay beamsteering receiver applications that require a large bandwidth [6]. The simulated single ADC achieves 17.7 fF/conv-step at 250 MS/s and the TI ADC at least 47.6 fF/conv-step at 2 GS/s.

II. SAR ADC WITH OVERLAPPING CONVERSION STEPS

The concepts of non-overlapping and overlapping conversion steps are presented in Fig. 1. SAR ADC sample rates are generally limited by the delays and settling times of the constituent DAC, comparator and SAR. Conventional SAR ADCs solve the digital code one bit at a time, meaning that several conversion steps must fit the conversion window, depending on the resolution. The DAC, comparator and SAR are activated sequentially during each step and they have maximum allowable delays and settling times as the output of each component must stabilize to the correct value before it is used by the next. Increasing the sample rate or sampling clock duty cycle reduces the conversion window and thus tightens the delay requirements.

Fig. 1. Concept of overlapped conversion timing compared to conventional timing for a 9-bit ADC.
Fig. 1 shows how the delay requirements may be alleviated by overlapping consecutive conversion steps. Conventionally, the steps are separate. A bit is first preset (p) in the SAR, then solved (s) by the comparator, and finally updated (u) to the SAR as the next bit is preset. This process is repeated $N$ times to solve $N$ bits. Each step may be done over two clock cycles so that the next bit is preset at the time when the previous is solved, overlapping two steps and using a total of $N+1$ clock cycles for the conversion. The maximum allowable delays are shown in the figure: $t_1$ is the sum of SAR clock-to-Q delay, DAC control delay and DAC settling delay, and $t_2$ the sum of comparator delay and SAR setup time. The same delays are summed in $t_3$, however since the comparator and SAR are triggered at the same time, the smaller of the corresponding delays is eliminated from the sum. Assuming equal conversion time ($t_{\text{conversion}}$), the improvement in maximum delays may be calculated for an $N$-bit ADC as

$$
\frac{t_3}{t_1} = \frac{t_3}{t_2} = \frac{t_{\text{conversion}}/(N+1)}{t_{\text{conversion}}/2N} = \frac{2N}{N+1}. 
$$

Thus the delay requirements are relaxed and the sampling rate could be increased accordingly.

Implementing overlapped conversion steps requires little additional hardware. One multiplexer per bit is added between the SAR and the DAC that selects if the DAC control signals are derived from the comparator or the SAR; the bit is taken from the SAR before and after the second clock cycle and from the comparator during the second cycle.

III. PROPOSED ADC

In this paper, an 8-way time-interleaved SAR ADC that overlaps some conversion steps is implemented. Fig. 2 shows the block diagram of the ADC. In addition to the basic CDAC, comparator and SAR that sample and quantize the signal, each ADC contains a tunable delay line for skew compensation, clock generator, output register and CDAC control logic circuit. A reference clock that determines the operating speed is given to the delay line that cancels delay differences between the clock source and the ADCs. The delayed clock is used to clock the digital parts in addition to being the reference from which other clocks are derived. In the process of generating the other clocks, the clock generator produces a set of one-hot enable signals that are used to control the SAR and CDAC control logic. The control logic implements overlapping conversion steps and converts the 9-bit SAR code to 26 control bits required by the CDAC. After all bits have been solved, the output register captures the result and keeps the ADC output constant during the next conversion.

Fig. 3 shows the timing diagram of the proposed ADC. Single ADC clock waveforms are displayed with solid lines and additionally the time-interleaved sampling clocks of the other ADCs with dashed lines. The sample clock duty cycle was required to be a low 1/16 by the application; this ADC was designed to be integrated to a 2 GHz RF bandwidth true-time-delay beamsteering IQ receiver front-end where the delay is implemented using a sample-resample procedure, and the steering range would have been limited by a large duty cycle [6]. The ADC was required to generate the needed clocks, thus a digital clock with a frequency of 16 times the single ADC sampling frequency is used as a reference. This clock also controls the SAR, i.e. the preset and update operations, and the comparator clock gated from it controls the solve operation. The five most significant bits (MSB) are solved with conventional timing where the conversion steps are separate, and the four least significant bits (LSB) are solved using overlapping to fit the remaining steps to the conversion window. After all bits are solved, the code is saved to the output register. The LSB is not updated in the SAR as it can be written directly to the output register to avoid an additional clock pulse. By overlapping some steps, the total conversion time is reduced to 83% of the reference conversion time without overlapped steps. Only four LSB steps are overlapped in this design to minimize the complexity of the clock generator.

A. Clock Generator

Fig. 4 shows the clock generation circuitry. The core of the generator is a synchronous 4-bit counter that can be reset to a configurable value. After resetting, the counter starts incrementing its output from the reset value with a frequency determined by the digital clock. For time-interleaved operation, the clock generators of different ADCs are initialized to values that are two-apart, i.e. ADC 1 is set to 14, ADC 2 to 12, ADC 3 to 10 and so on. The output clock is generated by
inverting the MSB of the counter. Other timing related signals are derived by converting the counter bits to a 16-bit one-hot bus. This bus is used to preset and update the SAR bits and one of the signals is used as the sampling clock. It is also used to derive a clock enable signal that gates the digital clock, yielding the comparator clock with nine pulses per conversion.

B. SAR

The clock generator is closely related to the SAR whose schematic is presented in Fig. 5 (a). The SAR consists of one D flip-flop (DFF) per bit and combinational logic controlling the inputs of the DFFs. Each SAR segment has several inputs that are used to time the conversion of the corresponding bit. Reset sets the bit to 0, preset to 1 and update to the comparator output value on the next rising edge of the digital clock. If none of the signals are high, the DFF retains its value via a feedback loop. The MSB only needs to preset and update and the LSB only to reset and preset during conversion, which results in reduced complexity for these bits. The reset, preset and update signals are some of the one-hot enable signals taken from the clock generator.

The proposed synchronous SAR reduces the preset delay and more than halves the update delay comparing to the commonly used asynchronous design shown in Fig. 5 (b) [7]. The figure shows the path from clock to output in orange when presetting a bit and in red when updating the bit. The preset and update delays can be calculated as

\[
\Delta t_{\text{preset}} = \Delta t_{\text{clk}} - Q + \Delta t_{\text{set}} \tag{2}
\]

\[
\Delta t_{\text{update}} = 2\Delta t_{\text{clk}} - Q + \Delta t_{\text{set}} \tag{3}
\]

where \(\Delta t_{\text{clk}} - Q\) is the DFF clock-to-Q delay and \(\Delta t_{\text{set}}\) the asynchronous set delay. For the proposed SAR the delay path is shown in green and the delays are

\[
\Delta t_{\text{preset}} = \Delta t_{\text{update}} = \Delta t_{\text{clk}} - Q. \tag{4}
\]

Therefore the delays are reduced and the proposed SAR is more suitable for high speeds.

C. CDAC

Fig. 6 (a) shows the one-sided simplification of the CDAC. This design uses a common mode voltage (VCM) based split capacitor array that samples the analog input directly to the DAC capacitors. The CDAC is split to 4-bit MSB and LSB subarrays via a bridge capacitor. The VCM-based design has capacitors only for bits 7 to 0 as the MSB capacitor is replaced with an additional reference voltage that is the average of the positive and negative references. To maximize the full-scale range of the ADC, the positive reference is fixed to the analog supply voltage and negative to ground. Splitting the CDAC and removing the MSB capacitor results in a total sampling capacitance of 31 unit capacitances per side, whereas the conventional binary-weighted 9-bit CDAC would have 512 unit capacitances per side, and thus a reduction of 94% in the number of unit capacitors is achieved.

Each capacitor in the CDAC consists of one or more parallel unit capacitor circuits shown in Fig. 6 (b). Unit capacitors are used to enable common centroid layout that reduces mismatches. Each unit capacitor has a bootstrapping circuit that boosts the sampling clock to eliminate signal dependent switch resistance, improving linearity. The unit capacitors are connected to reference voltages using switches that are controlled by the SAR or comparator. A large unit capacitance of 62 fF was chosen to reduce the effect of mismatches and parasitics that degrade the accuracy especially in split CDACs. Metal-oxide-metal capacitors with minimal breakdown voltage were used to keep the ADC area small.

Additional logic is required on the feedback path from digital to analog side as each CDAC bit requires three control signals while the SAR has only a 9-bit output. Fig. 6 (c) shows how two bits are used to generate the MIN, CM and MAX signals that connect capacitors to references as in Fig. 6 (b). One of the bits is the MSB stored in the SAR and the other depends on the capacitor. For the non-overlapping bits the bit is the corresponding SAR bit, and for the overlapping bits it is taken from a multiplexer that chooses between the SAR bit.
and the comparator output.

IV. SIMULATION RESULTS

The proposed ADC was implemented in 22 nm CMOS process and its functionality was verified in simulations. Fig. 7 shows the layout of one ADC as a part of the TI ADC which is created by stacking ADCs to a column and adding a synchronizer circuit that passes the data to RAM memory. Each ADC consumes 0.0085 mm$^2$ while the TI ADC consumes 0.088 mm$^2$.

The performance of the ADC was evaluated through simulations. Fig. 8 shows the near-Nyquist output spectrum of the single ADC and TI ADC at full scale 1.6 V peak-to-peak differential input with 1024 samples taken. Fig. 9 shows the SNDR and SFDR of both ADCs as a function of the input frequency. The single ADC SNDR is a stable 52 dB throughout the whole band, whereas the TI SNDR drops from 52 dB at low frequencies to 48 dB near Nyquist due to limitations in the sampling circuit. At 0.8 V VDD and 0.4 V VCM, the single ADC consumes 1.43 mW at 250 MS/s and the TI ADC 19.8 mW at 2 GS/s. The power of different subcircuits is shown in Fig. 10. Most of the power in the single ADC is used by the clock generation circuitry, whereas for the TI case skew-compensating delay lines are required and these consume most power. The Walden figure-of-merit for the single ADC is 17.7 fJ per conversion step for both low and high signal frequencies, and for the TI ADC 29.7 fJ/conv-step and 47.6 fJ/conv-step at low and high frequencies respectively. Table I compares the simulation results to the measured results of some state-of-the-art designs. The results are promising and show that the ADC could perform highly in measurements.

V. CONCLUSION

This work presented a 2 GS/s 8-way time-interleaved 9-bit SAR ADC design that overlaps conversion steps to improve the sample rate. The SAR speed is enhanced using synchronous clocking that is enabled by a clock generator that controls the conversion timing. The CDAC uses a VCM-based split array to achieve high speed and low power. The functionality of the ADC was verified through simulations where the single ADC achieves Walden figure-of-merit of 17.1 fJ/conv-step and time-interleaved ADC 47.6 fJ/conv-step.

<table>
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<th>TABLE I COMPARISON TABLE</th>
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<td>FOx [fJ/conv-step]</td>
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REFERENCES


